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Variable-frequency pulse-width-modulation for zero-voltage switching in a boost DC-DC regulator

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Variable-Frequency Pulse-Width-Modulation
For Zero-Voltage Switching in a
Boost DC-DC Regulator

by

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Thesis Advisor: Dr. Gerald D. Ewing

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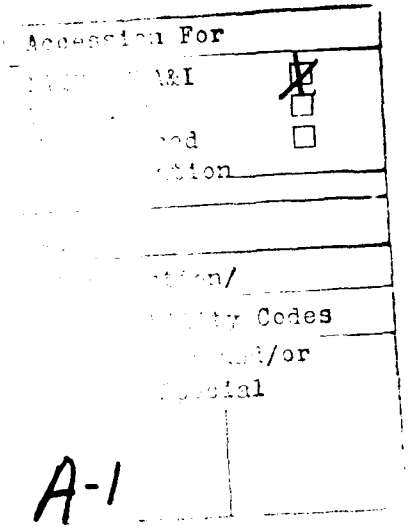

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Variable-Frequency Pulse-Width-Modulation
For Zero-Voltage Switching in a
Boost DC-DC Regulator

by

Daniel Scott Hunter
Lieutenant, United States Navy
B.S., Pennsylvania State University, 1982

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ABSTRACT

A technique for operating a pulse-width-modulated (PWM) dc-dc regulator in the boost mode while switching the MOSFET when the drain-to-source potential is near zero volts was developed and is described in this thesis. This is accomplished by using frequency-modulation in addition to pulse-width-modulation. Zero-voltage switching will provide power converter designers an alternative for designing high-frequency converters with minimal transient turn-on losses, the predominant form of converter losses experienced in high frequency operation. High frequency operation will result in smaller reactive components, which produce higher power density converters, as well as increasing the transient response of the regulated converter. In addition to allowing for high frequency operation, the design exhibits many desirable power switch properties, such as limiting the peak voltage to the output voltage level and operating with the minimum possible current levels for a given power requirement. A circuit built and tested utilizing zero-voltage switching in a regulated boost converter verified the principles of operation for yielding a high-efficiency, high-frequency converter.

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ACKNOWLEDGEMENTS

Zero-voltage switching in the PWM boost converter was first developed and analyzed by Dr. Gerald D. Ewing as a solution to a control problem I was having in the design of another PWM circuit. His insight into solving problems, synthesizing new circuit ideas and analyzing them in power electronics has opened new areas of research into high-frequency converters. In addition, his suggestions on circuit layout and noise reduction were instrumental in obtaining a high quality power converter design.

I would also like to thank my wife, Cathy, and son, Matthew, for their support throughout this project.

I. INTRODUCTION

Non-dissipating regulated power converters fall into two general categories, pulse-width-modulation and resonant (or quasi-resonant) frequency-modulation. The difference between the two modulation schemes is whether the device is operated in a constant-frequency variable pulse-width mode (PWM) or in a constant pulse-width variable-frequency mode. This thesis combines the two topologies into a single variable-frequency variable pulse-width converter to obtain a regulated zero-voltage switched dc-dc boost converter.

The ability to switch under a zero drain-to-source potential will allow the basic PWM converter to attain switching frequencies in the range of several megahertz without undergoing turn-on losses in the switch. The motivation for operation at higher frequencies is that, as frequency increases, the energy storage elements in the converter become smaller and the converter can be packaged in a smaller volume. In addition, the higher frequencies increase the transient response of the regulated converter. Losses are generated when the energy stored in the drain-to-source capacitance of the MOSFET is dissipated at turn-on. For a typical circuit capacitance of 200 pF, a power switch operating at 1 MHz boosting in a discontinuous mode from 150 volts to 300 volts could be expected to dissipate 2.25 watts. For operations in the 5 MHz range, power dissipation could exceed 12.5 watts. For continuous mode regulators, losses would be 9 and 45 watts respectively. This level of power dissipation cannot be tolerated in an efficient converter.

When the switch is turned on under a zero-voltage condition, the energy stored in the MOSFET's drain-to-source capacitance is zero. The predominant

switch losses under this condition are turn-off losses and conduction losses. The turn-off losses that occur in the device are due to the current flow in the switch not attaining a zero level prior to the voltage across the switch rising. This loss can be minimized by ensuring that the channel current reaches zero before the voltage level across the device rises appreciably. This is accomplished by choosing a device with a high transconductance value and driving it with a fast fall-time gate-source pulse. The conduction losses can only be reduced by choosing a device with a low drain-to-source channel resistance. In general, the MOSFET channel resistance increases with increased voltage capability and decreases with increased current capability; however, devices with higher current capabilities tend to provide higher drain-to-source capacitances. A design tradeoff must be made between the capacitive effects of the junction and the junction's channel resistance.

In addition to the elimination of capacitive turn-on losses, zero-voltage switching also provides the following benefits [Ref. 1:pp. 116-117]:

- Turn-on with zero voltage avoids the switching Miller effect. Side effects of the Miller effect include current spikes in the gate drive, higher gate drive switching losses, slower turn-on speed, severe EMI and noise generation.
- The elimination of the switching Miller effect greatly simplifies the design of gate drive circuitry and gate drive power and current requirements.
- The body diode in the MOSFET design is utilized for conduction in the reverse direction, clamping the voltage at a near zero value.

A zero-voltage switched variable-frequency PWM converter was designed and tested. The device operated at a nominal 67 kHz and 8 μs pulse-width for a regulated conversion of 35 volts to 94.7 volts, delivering 8.87 watts while operating at 93.5% efficiency. As the input voltage varied between 33.5 and

41.8 volts, the frequency ranged from 60 kHz to 80 kHz with pulse-widths ranging from 10 μs to 6 μs. The low operating frequency was chosen in response to the limitations imposed by the controller and to allow for accurate instrumentation.

A. OPTIMAL SWITCHING CHARACTERISTICS

Optimal power switch utilization is insured by meeting the following basic criteria:

- Turns on under zero voltage.
- Turns off under zero current.
- Minimum possible current to flow for given load requirements.
- Maximum voltage across the switch is minimized.
- Minimum peak-to-average current ratio through the switch.

As stated in the introduction, the ability to turn on under zero voltage allows the designer to operate at higher frequencies without turn-on losses in the switch. In addition, the gate drive power is markedly reduced because there is no Miller effect capacitance [Ref. 1:p. 117]. The zero-voltage switched quasi-resonant converter family and the variable-frequency PWM boost converter provide this switching characteristic.

The maximum voltage that is experienced across the switch in a zero-voltage switched quasi-resonant converter is over twice the output value for the boost converter. This requires that the switch be designed for the peak voltage vice the output voltage at a cost of increased channel resistance which results in increased conduction losses. In the PWM converter, the peak voltage seen by the switch is equal to the output voltage.

The ability to turn off under zero current allows the transient dissipation of the switch to be zero at turn-off because the product of voltage and current through the switch is zero when the switch is commutated. The converter designed and tested in this thesis does not possess the ability to turn off under zero current. It does, however, hold the switch voltage low for a longer period than normal for this type of converter. This allows the channel current to clear before the voltage rises appreciably, thereby reducing the amount of transient dissipation handled by the switch. The zero-current switched resonant converter family provides this type of characteristic for the different classes of converters.

The optimal waveform for transferring energy through a power switch is a square current waveform proportional to the required output current. The PWM converter utilizes a triangular-shaped current waveform with the peak value of current occurring at turn-off. The value of the peak current level is proportional to the required output current to supply the given load. The zero-current resonant converter family utilizes a half-sinusoid current waveform with constant amplitude, regardless of the magnitude of output requirements. The zero-voltage switched family of quasi-resonant converters yields a fairly square current pulse that is independent of load and is based on the maximum load requirement [Ref. 1:p. 73].

Of the properties that define optimal switch utilization, the dominant characteristic in limiting the operating frequency of a converter is the transient turn-on loss. The zero-voltage family of quasi-resonant converters and the variable-frequency PWM boost converter developed in this thesis are currently the only classes of converters that possess this capability. The advantage of the variable-frequency PWM boost regulator over the quasi-resonant boost regulator

is that the peak voltage across the switch is twice as high in the resonant converter than in the circuit described in this thesis. The peak current flow through the switch, however, is higher in the variable-frequency PWM converter, except at output power levels less then design maximum. Because current is proportional to output power in a PWM converter, it provides a lower peak current when operating at less then maximum power leveis.

B. ORGANIZATION

This thesis is organized according to the following criteria. The theoretical background required to perform the analysis is presented in chapter two. Chapter three involves the actual circuit design that was performed in the experiment. Chapter four gives the results of the experiment and chapter five discusses conclusions that are based on the research performed.

II. THEORETICAL BACKGROUND

The ability to operate the device under a zero drain-to-source potential during turn-on is obtained by exploiting the parasitic resonance that is inherent in all discontinuous PWM boost converters. This resonance is obtained from the transfer of power from the parasitic capacitance that is present in the pass diode, the MOSFET and the inductor back into the circuit's inductance when the energy that was present in the inductor had been transferred to the load. To obtain a true zero-voltage switching condition using the technique developed, it must be noted that the output voltage must be at least twice the input voltage. If this is not the case, then this technique can be implemented to provide a minimum voltage switched vice a zero-voltage switched converter. A basic schematic of a boost PWM converter is shown in *Fig. 1.*

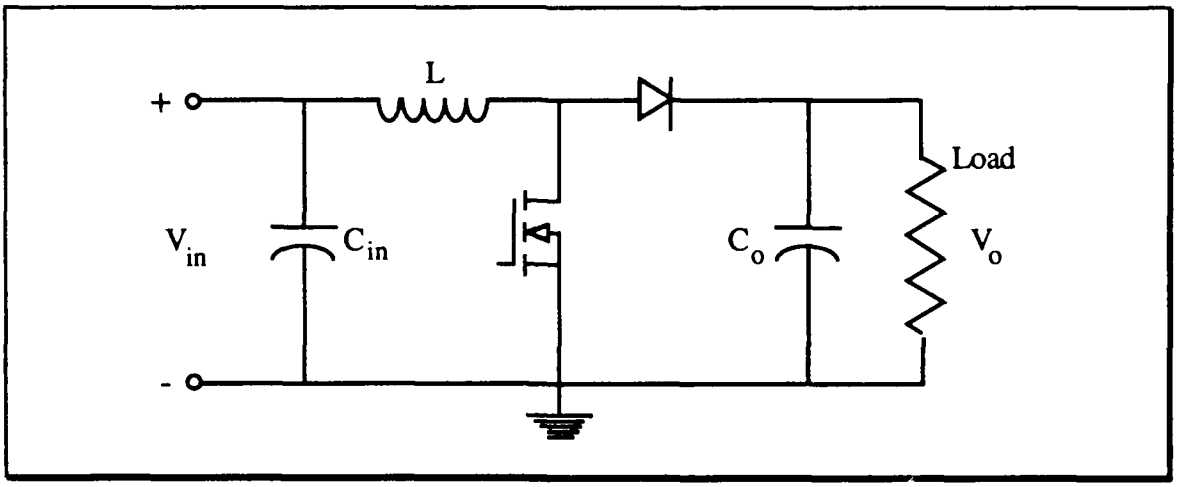

Figure 1. Boost converter schematic

A. BOOST CIRCUIT ANALYSIS

The ideal boost PWM circuit operates in three basic steps shown in Fig. 2. These steps are basically defined as:

- Inductor charge stage. During this time period, the power switch is closed and the inductor current rises linearly to a maximum level at turn-off.
- Inductor discharge stage. The power switch is opened, the inductor voltage polarity switches and rises to the difference between the input and output voltage level and discharges the stored energy into the load. At this time, the input is also supplying energy to the load.
- Dead time. The inductor has been depleted of its energy and the switch is still open. The pass diode blocks current flow from the output filter capacitor from going back into the source.

Each of these three phases are described by the current and voltage relationships at the inductor and the power switch. During the period when the switch is closed, the current through the inductor will rise linearly to a level defined by the applied input voltage and the circuit impedance. The voltage across the inductor is approximately equal to the input voltage and the switch potential is negligible.

When the control loop removes the gate drive pulse, the switch opens and the voltage across the inductor rises to a level such that it will forward bias the pass diode and pass energy to the load. The voltage across the inductor is the difference between the output voltage and the input voltage, and the switch potential rises to the output voltage level.

The energy that is stored in the inductor during the time the switch is closed will be depleted and the diode will block the back flow of current from the output into the input. At this time, the current through and the voltage across the

inductor is zero with the voltage across the switch at the input voltage level. The controller then applies a gate drive voltage and the cycle is repeated.

The voltage and current waveforms for the inductor and switch are presented in Figs. 3 and 4 with the gate drive being represented in part (a) and the current and voltage in parts (b) and (c) respectively.

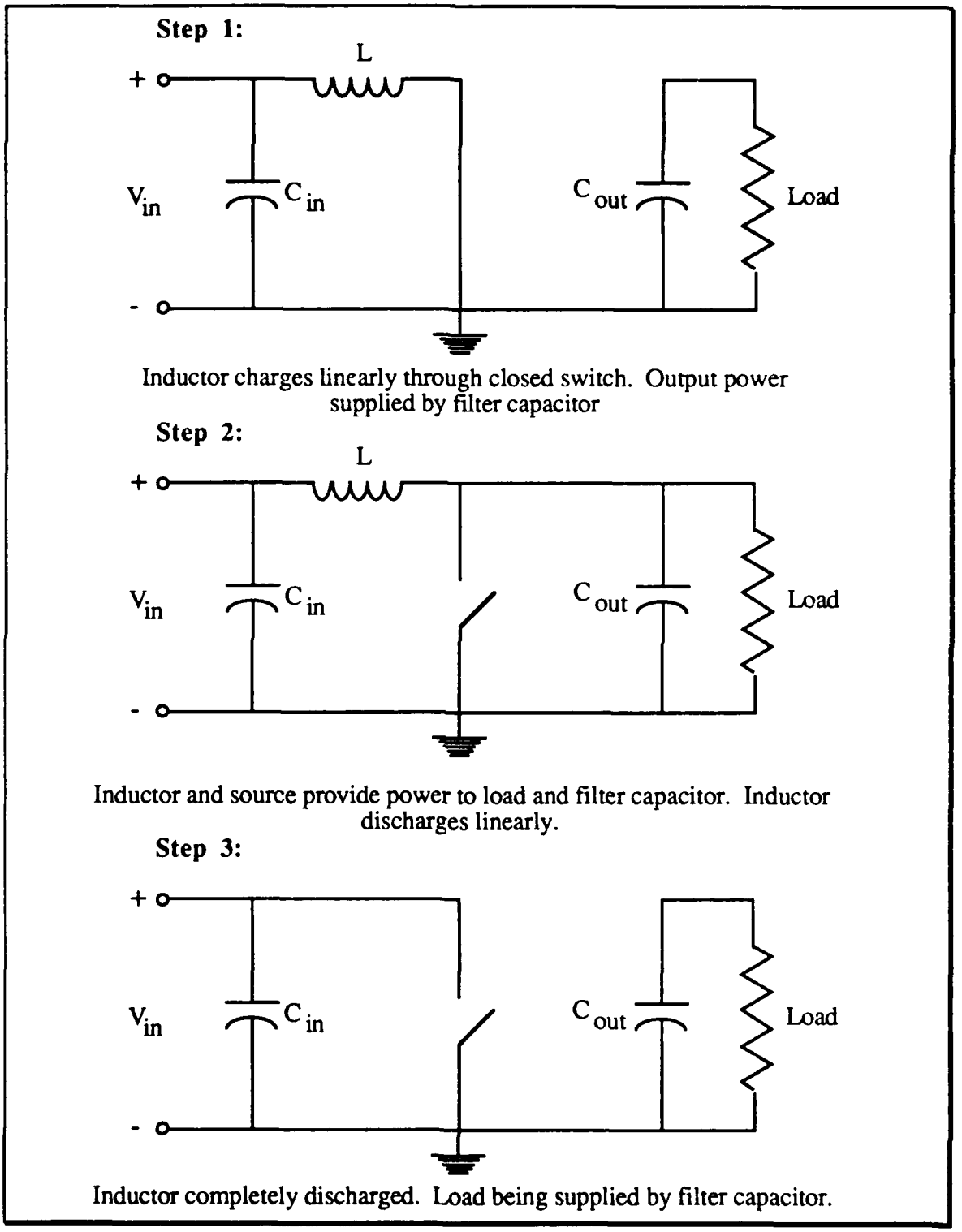

Figure 2. Equivalent circuit diagram for three stage boost circuit

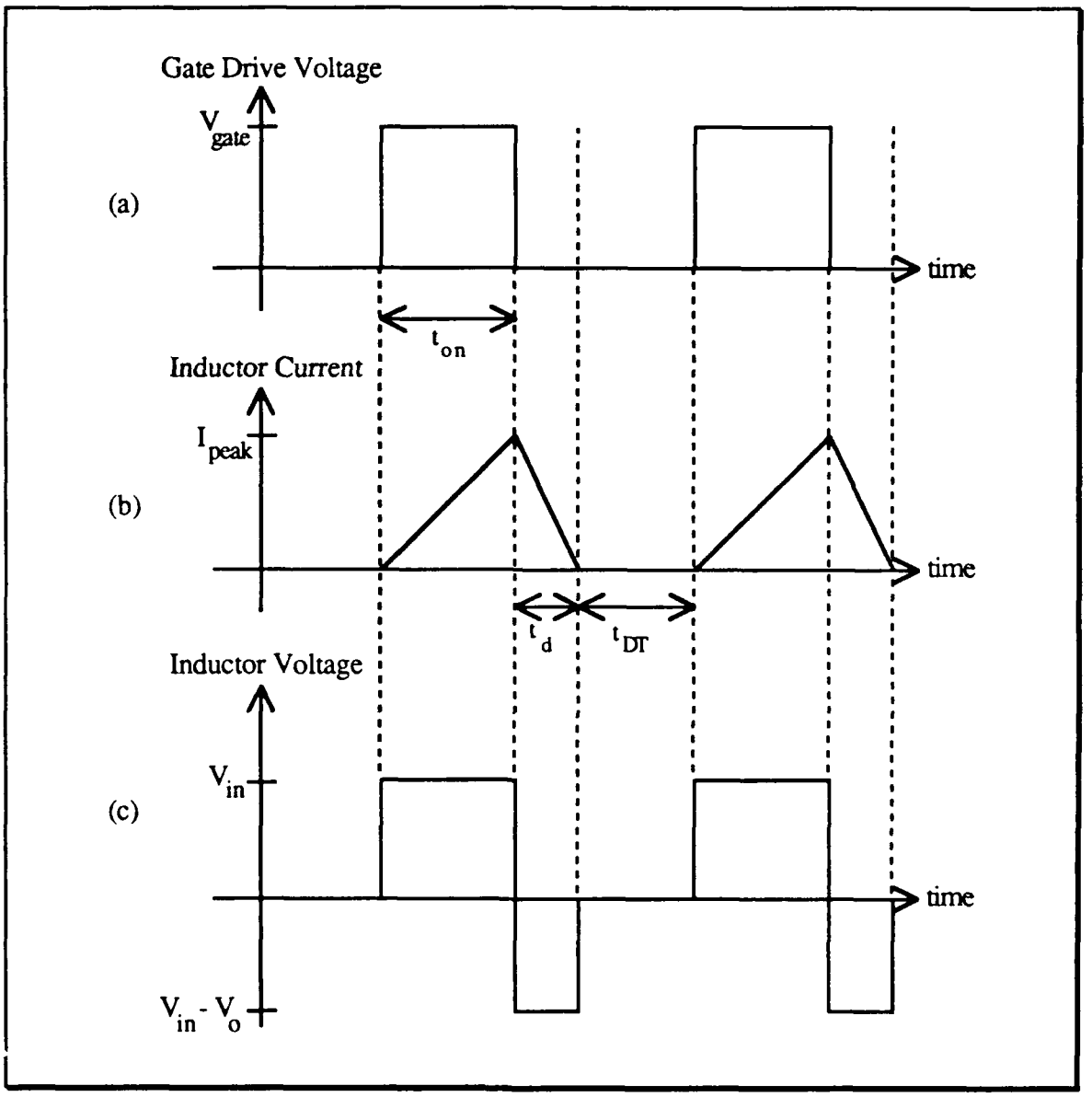

Figure 3. Inductor waveforms

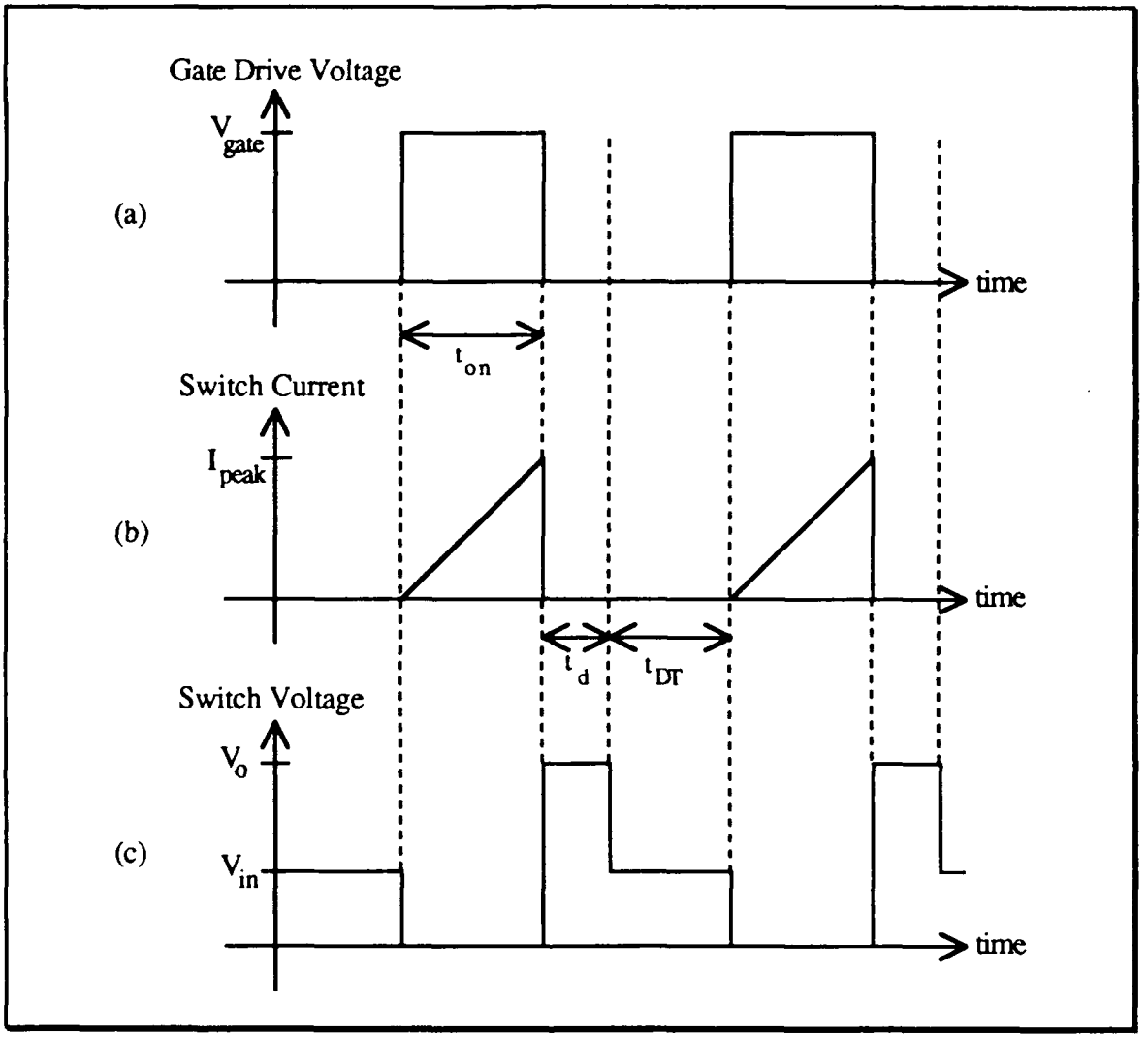

Figure 4. Switch waveforms

The amount of energy that is transferred to the output is dependent on the amount of time that the switch is closed, called the pulse-width, and the amount of time required to discharge the inductor. Faraday's law states that the volt-second product of the inductor must be equal for both the charge and discharge cycles. If the time to charge the inductor is called t_{on} and the discharge time is called t_d, then the volt-second product of the inductor is written

$$V_i t_{on} = (V_o - V_i) t_d . \qquad (1)$$

Solving the equation for the voltage conversion ratio, $\frac{V_o}{V_i}$, one obtains,

$$\frac{V_o}{V_i} = \frac{t_{on} + t_d}{t_d} \quad . \tag{2}$$

Replacing the times by a normalized value d, where d_1 is the ratio of the on-time to the total switch period and d_2 is the ratio of the discharge time to the total switch period, then

$$\frac{V_o}{V_i} = \frac{d_1 + d_2}{d_2} \quad . \tag{3}$$

The voltage conversion ratio can also be expressed as a function of the output load. As the boundary conditions on the inductor are equal for both charge and discharge periods, i.e., they both have a peak value of I_p and a minimum value of zero, then the average current for both periods are equal. The average current through the inductor is one half of the peak value since it is triangular in shape. The peak value of the current occurs at the end of the on period and is given by

$$I_p = \frac{V_i t_{on}}{L} \tag{4}$$

resulting in an average current during charge of

$$I = \frac{V_i t_{on}}{2L} \quad . \tag{5}$$

The average current during discharge is given by

$$I = \frac{V_o}{R} \frac{T}{t_d} \tag{6}$$

where R is the load resistance and T is the total switch period. Equating equations (5) and (6) yields a voltage conversion ratio of

$$\frac{V_o}{V_i} = \frac{t_{on} t_d R}{2LT} = \frac{d_1 d_2 TR}{2L} \quad . \tag{7}$$

This equation is used for determining the range of values for which the converter will operate in the discontinuous mode, and is used for determining the proper size inductor for a given load to maintain regulation at the desired operating frequency.

B. ZERO-VOLTAGE SWITCHED BOOST CONVERTER

For a non-ideal converter, parasitic capacitance is present in the pass diode, the MOSFET, and the inductor, and stray inductance is present throughout the circuit in addition to the inductance used in the converter. The parasitic elements along with the device elements cause the ideal waveforms to vary during the transitional periods of switch activity. To do a complete analysis on the boost cycle, the cycle is divided into five distinct times defined by the switch potential. These periods are called the on-time, rise-time, discharge time, resonant ring-down time and the body diode conduction time. Figure 5 illustrates the time periods that are discussed.

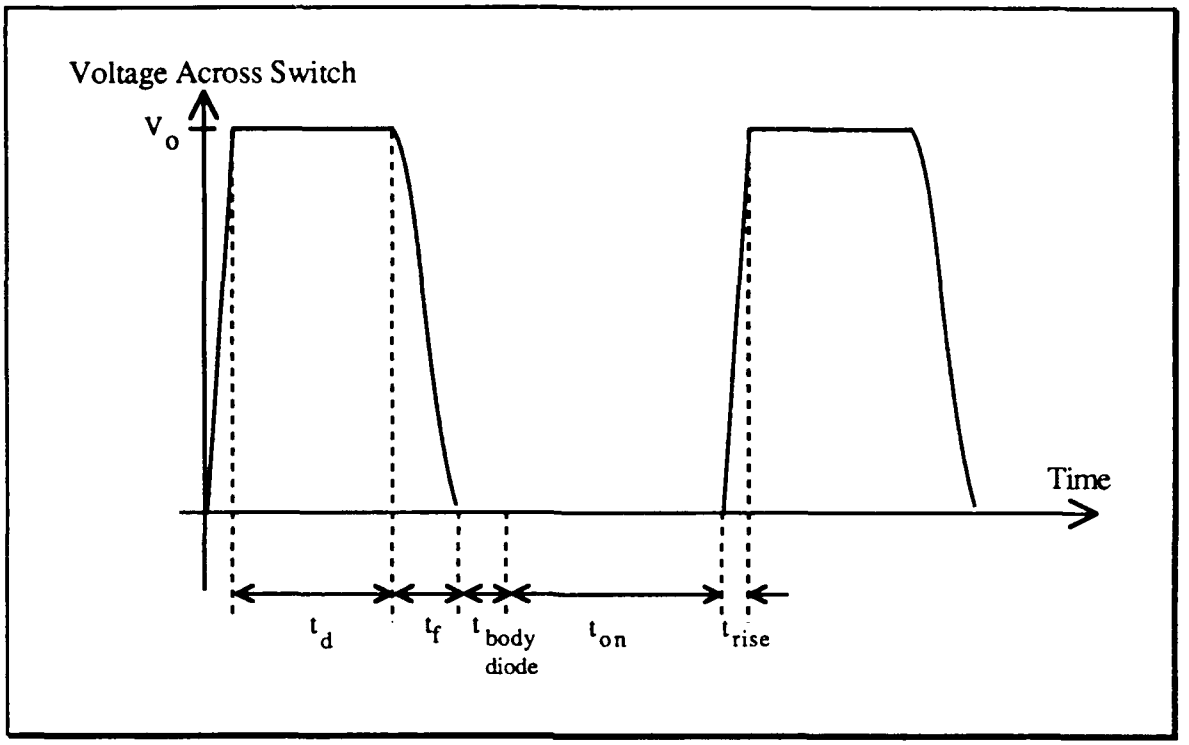

Figure 5. *Zero-voltage switching waveform*

1. Waveform Timing

The primary difference between the zero-voltage switching technique developed in this thesis and the standard analysis is that the dead time normally associated with the control loop is altered by external circuitry to cause the cycle to restart when the switch potential falls to zero. In an ideal boost circuit, the switch voltage falls to the input level after the inductor has released its energy. In the case where the parasitic elements play a part in determining the waveform, the voltage across the switch will fall below the level of the input voltage and resonate in a damped sinusoidal manner.

The level to which the voltage falls is determined by the difference between the input and output voltage levels. In the case of the zero-voltage switched converter, the output voltage level must be at least twice the input

voltage. In general, when the resonant ring-down period commences, the switch voltage will drop to the value

$$V_{sw} = 2V_{in} - V_{out} . \tag{8}$$

When the MOSFET is used as the switching device, the body diode will clamp the voltage at a slight negative value maintaining the switch potential near zero volts. If a bipolar device is used, an anti-parallel diode is required with the switch to allow the voltage to be clamped near the zero level.

a. On-time

The fraction of time that the switch is on relative to the total period establishes the output voltage level. It is usually chosen by the designer to be within a range of values such that expected load changes in the output or varying input voltages have minimal effect on the ability of the converter to stay in regulation. As will be discussed, the period of time that the switch is on is critical in the design of a zero-voltage switched boost regulator due to the current technological limitations on PWM regulator circuits.

The energy stored in the inductor during the switch's on period is given by

$$E_L = \frac{1}{2} L I_p^2 \tag{9}$$

where I_p is the peak current in the inductor. The charging current during this period is linear, and the peak value of current is determined from

$$v = L \frac{di}{dt} . \tag{10}$$

The peak current will occur when the switch is opened, where the total on time is defined as t_{on}. The peak current is expressed as

$$I_p = V_i \frac{t_{on}}{L} . \tag{11}$$

Substituting into equation (9), the inductor energy is

$$E_L = \frac{V_i t_{on}^2}{2 L} . \tag{12}$$

This energy in combination with the input supply are the sources of power for the load during the inductor discharge period.

b. Rise-time

The period of time from the opening of the switch to the point where the switch potential has reached its maximum is called the rise-time. This time is characterized by closing the MOSFET drain-to-source channel against a flow of current. This current must be re-routed through the pass diode and transferred to the load. It is at this time that transient turn-off dissipation occurs as the switch potential rises while a current flow still exists in the channel.

The rise in potential of the switch is synonymous with a rise in the drain-to-source capacitance voltage. The energy stored in the inductor during the period the switch is on is much greater then the energy required to charge the parasitic capacitance to the output voltage,

$$\frac{V_i t_{on}^2}{2L} > \frac{1}{2} C V_o^2 . \tag{13}$$

The inductor acts as a constant current source during this short time period following turn-off such that the relationship between the peak value and the time involved is written as

$$I_p \approx C \frac{V_o}{t_r} \quad . \tag{14}$$

Substituting equation (11) into equation (14), the rise-time for the switch drain-to-source potential is given as

$$t_r \approx \frac{LC}{t_{on}} \left(\frac{V_o}{V_i} \right) . \tag{15}$$

c. Discharge Time

The discharge time in the cycle is defined as the time required for the inductor to release its energy to the load. The length of time for this discharge is determined by the energy level in the inductor and by the input and output voltages. This discharge occurs linearly starting from the peak value of the inductor current at turn-off to a zero current level at the end of the period. During this time period, both the inductor and input supply energy to the load.

During the discharge period, the voltage across the inductor will equal the difference between the output and input voltage, and the drain-to-source potential will rise to the full output voltage. Using the basic inductor voltage-current relationship, the discharge period is given by

$$t_d = \frac{V_i \, t_{on}}{V_o - V_i} = \frac{L \, I_p}{V_o - V_i} \quad . \tag{16}$$

d. Resonant Ring-Down Time

The resonant ring-down portion of the cycle is critical in employing the zero-voltage switching technique. The resonant structure of the time period is a result of the circuit's parasitic capacitance, added capacitance and inductance throughout the circuit. The equivalent circuit at resonant ring-down is presented in Fig. 6.

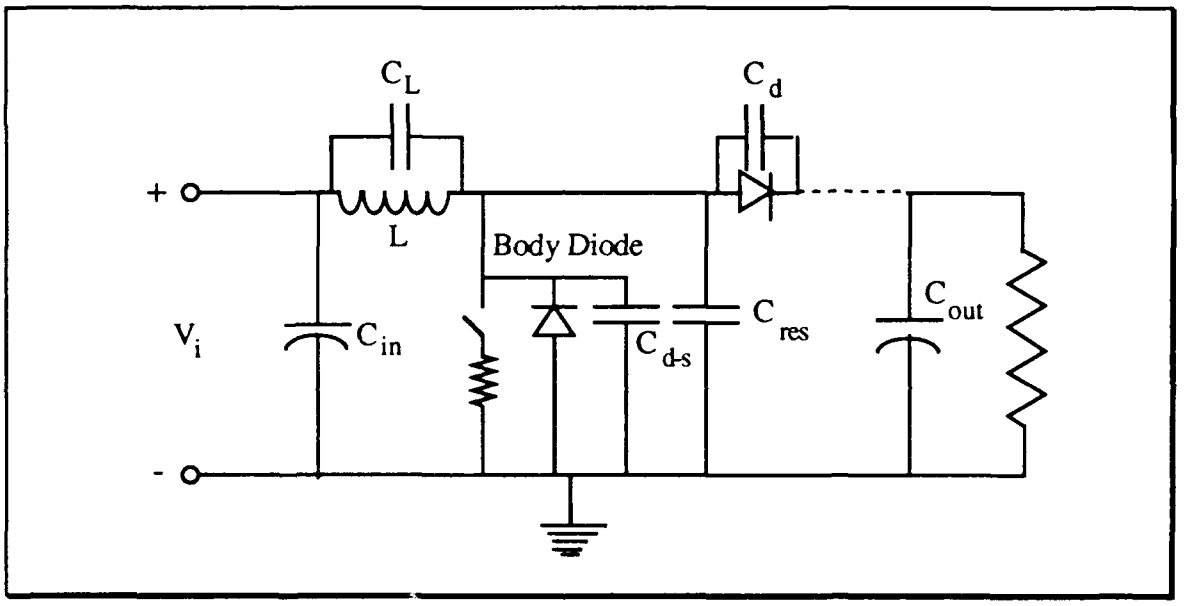

Figure 6. Equivalent circuit during ring-down

For the zero-voltage switching converter, the resonant ring-down period ends when the drain-to-source potential reaches zero. At this point, the body diode will start conduction and clamp the voltage near zero volts. The initial condition on the equivalent circuit capacitance is a charge of V_o volts. The charge on the capacitor will act to supply the circuit's inductance with current determined by

$$v_L = L \frac{di_c}{dt} \ , \ i_c = C \frac{dv_c}{dt} \qquad (17)$$

and

$$V_i = v_L + v_c\,, \tag{18}$$

where C is the equivalent circuit capacitance. Combining equations (17) and (18) with the initial condition in a Laplacian form, the s-domain capacitor voltage becomes

$$V(s) = V_o \frac{s}{s^2 + 1/LC} + V_i \frac{1/LC}{s(s^2 + 1/LC)}\,. \tag{19}$$

The capacitor voltage in the time domain is given by

$$v_c(t) = (V_o - V_i) \cos\left(\frac{t}{\sqrt{LC}}\right) + V_i\,. \tag{20}$$

The inflection point of the capacitance voltage, as well as the mean value, is at the level of the input voltage.

The time at which the body diode starts to conduct is determined by setting v_c equal to zero. This time is given by

$$t_f = \sqrt{LC}\left[\frac{\pi}{2} + \sin^{-1}\left(\frac{V_i}{V_o - V_i}\right)\right]. \tag{21}$$

The cosine function has been replaced by the shifted sine function to ensure that future calculations requiring this value are returned in the proper quadrant.

e. Body Diode Conduction Time

The conduction period of the body diode is determined by allowing the inductor, which has been resonating with the circuit's equivalent capacitance through the input source, to release its energy after the voltage across the switch

forward-biases the body diode. The discharge of the inductor at this stage is linear with the same slope as the charge portion of the cycle.

The current level when the body diode becomes forward biased is obtained from differentiating equation (20), substituting the time that the conduction begins from equation (21) and multiplying the result by the effective circuit capacitance, yielding

$$I = -\sqrt{\frac{C}{L}}(V_o - V_i)\sin\left(\frac{\pi}{2} + \sin^{-1}\left(\frac{V}{V_o - V_i}\right)\right). \tag{22}$$

To determine the amount of time that it will take the inductor to discharge, the basic inductor voltage-current relationship is used,

$$V_i = L\,\frac{I_{bd}}{t_{bd}}, \tag{23}$$

where I_{bd} is the magnitude of the body diode peak current level and t_{bd} is the time required to discharge the stored energy. When the output voltage is less then twice the input voltage, then I is greater than zero. When the output voltage is greater than twice the input voltage, then I is less then zero.

Solving equation (23) for the body diode conduction time yields

$$t_{bd} = \sqrt{LC}\,\frac{V_o - V_i}{V_i}\,\sin\left(\cos^{-1}\left(\frac{V_i}{V_o - V_i}\right)\right)$$

$$= \sqrt{LC}\sqrt{\left(\frac{V_o}{V_i}\right)^2 - \frac{2V_o}{V_i}}\ . \tag{24}$$

The zero-voltage switching requirement of turning the switch on when the switch potential is at or near zero volts requires that the PWM controller turn the switch on during this period.

2. Power Transfer

Power transfer from the input to the load takes place during the discharge cycle of the inductor through the pass diode. The energy that is supplied to the load is a combination of energy stored in the inductor and the energy transferred from the source in that time frame. The input power and the output power are equal in a lossless converter,

$$P_i = P_o = \frac{E_L}{T} + \frac{1}{T}\int_0^{t_d} V_i\, I_p\left(1 - \frac{t}{t_d}\right)dt$$

$$= \frac{LI_p^2}{2T} + \frac{V_i I_p t_d}{2T}, \qquad (25)$$

where the discharge time is given by equation (16), which yields

$$P_o = \frac{LI_p^2}{2T}\left[\frac{V_o}{V_o - V_i}\right]. \qquad (26)$$

Substituting the value for the peak current in the inductor, equation (11), the power transferred to the load is

$$P_o = \frac{V_i^2\, t_{on}^2}{2LT}\left[\frac{V_o}{V_o - V_i}\right] \qquad (27)$$

where T is the total length of time for one complete cycle. This time is given by the sum of all conduction times in the circuit,

$$T = t_{on} + \frac{LC}{t_{on}}\frac{V_o}{V_i} + \frac{V_i}{V_o - V_i}\, t_{on} +$$

$$\sqrt{LC}\left[\frac{\pi}{2} + \sin^{-1}\left(\frac{V_i}{V_o - V_i}\right)\right] + \sqrt{LC}\sqrt{\left(\frac{V_o}{V_i}\right)^2 - \frac{2V_o}{V_i}}. \qquad (28)$$

Using equations (27) and (28), one can obtain the required values for the inductance and circuit capacitance to obtain a power level at a desired output voltage and operating at a desired frequency.

The response to a change in output power requirement on the pulse-width is determined to a first approximation by neglecting the terms in the total period that are of short duration. The primary terms in the power transfer equation are the switch on-time and the inductor discharge time. Setting all other components of equation (28) to zero and substituting into equation (27), the output power is determined by

$$P_o = \frac{V_i^2 t_{on}}{2L\left(1 + \frac{V_i}{V_o - V_i}\right)}\left[\frac{V_o}{V_o - V_i}\right] . \tag{29}$$

Differentiating the output power with respect to the time the switch is on yields

$$\frac{dP_o}{dt_{on}} = \frac{V_i^2}{2L\left(1 + \frac{V_i}{V_o - V_i}\right)}\left[\frac{V_o}{V_o - V_i}\right], \tag{30}$$

which illustrates that changes in output power are directly proportional to changes in the pulse-width of the converter.

3. Dissipation Analysis

Transient dissipation in the zero-voltage switched converter is limited to turn-off transients. Turn-off transients are a result of the channel voltage rising while current is flowing through the channel. Techniques have been developed for dissipating the turn-off energy in a PWM converter outside of the switch,

such as turn-off snubbers, and are either dissipating or non-dissipating in their energy removal techniques.

The technique of transient dissipation suppression used in this circuit involves utilizing the extra capacitance, placed in the circuit to provide the required ring-down time, as a means of holding the drain-to-source potential at a low level while the channel clears of current. The added capacitance serves to effectively bypass the current during the transitional period when the switch opens. The ability to measure the actual transient current through the channel is limited because the parasitic capacitance redirects the current flow from the channel during the transitional period.

The MOSFET's transconductance determines the rate at which the channel conduction varies when the gate signal is varied. In the switching mode of operation, the time required to close the channel is dependent on the rate at which the device's gate-to-source capacitance is discharged. During turn-off, the voltage rise across the channel takes a much longer period of time than the current drop through the channel. The dissipation that occurs during turn-off in the circuit during a complete switching cycle is given by

$$P_{turn\text{-}off} = \frac{1}{T}\int_0^{t_o} I_p \left(1 - \frac{t}{t_o}\right)\left(\frac{V_o}{t_r}\, t\right) dt \qquad (31)$$

where t_o is the time required to clear the channel and t_r is the time required for the voltage to rise from zero to the output voltage level. At time t_o, the current through the channel is zero and the power loss due to the transient switching action is zero. Solving the above yields

$$P_{turn\text{-}off} = \frac{I_p V_o t_o^2}{6Tt_r} \quad . \tag{32}$$

The effect of switching the device under a load is observed in the gate drive circuitry and in the added noise observed in the current and voltage waveforms.

C. MOSFET

MOSFET devices are used in switch mode circuits for their ability to switch very rapidly. MOSFET switching devices have been used as power switches for speeds up to 10 MHz [Refs. 2, 3]. The MOSFET used in most power converter applications is an N-channel enhancement mode transistor where the body and source form an anti-parallel diode across the transistor. This anti-parallel diode is an integral part of the zero-voltage switched converter in that it holds the switch voltage near zero during the reverse conduction cycle of the MOSFET.

The MOSFET is a charge control device. The control voltage is applied to the gate of the device and induces an electric field across the dielectric barrier, usually SiO_2, and clears the channel to allow current to flow through the device [Ref. 4:p. 106]. This insulated gate structure gives the MOSFET a very high input impedance. In the switching mode, the channel is cleared and the device acts as a series resistance to current flow. The drain-to-source resistance, $R_{DS\text{-}on}$, is an important figure of merit for MOSFETs. This is a disadvantage when compared to the bipolar transistor because conduction losses can account for a significant portion of switch losses at high current levels. Advantages of the MOSFET include a small current drive requirement, that they do not display a second breakdown failure mode and that they display a stable switching time as

temperature changes [Ref 5:p. 12]. In addition, since the MOSFET is a majority carrier device, they do not require the elaborate reverse current circuits that are required for turning off bipolar power transistors. Upon release of the gate drive potential, the device begins to turn off immediately [Ref. 6:pp. 91-92].

Design considerations when using a MOSFET in a power switching circuit are twofold. First, the lengths of all leads going to the device must be minimized. This is especially true of the gate drive lead. Long leads in the gate drive circuitry will cause oscillations as the parasitic inductance and the MOSFET capacitance form a resonant network. If the leads are long, lossy ferrite beads or a small resistor in series with the drive can reduce oscillations. The second factor important in utilizing the MOSFET is due to the high input impedance of the MOSFET. This high input impedance requires that the driving source impedance be very small in order to prevent positive feedback in the drive circuit, which comes from the Miller effect discharge of the drain-to-source and gate-to-drain capacitance into the drive circuit during turn-off, leading to oscillations. [Ref. 6:p. 96]

D. MILLER EFFECT

The Miller effect of the MOSFET is a result of the insulated gate structure of the device. This structure yields a relatively high value of capacitance between the gate-to-drain and the gate-to-source junctions. The device's inherent depletion capacitance between the drain and source combines with the other capacitances to play an important role in the characteristics of the switching MOSFET. The model of the MOSFET is given in Fig. 7.

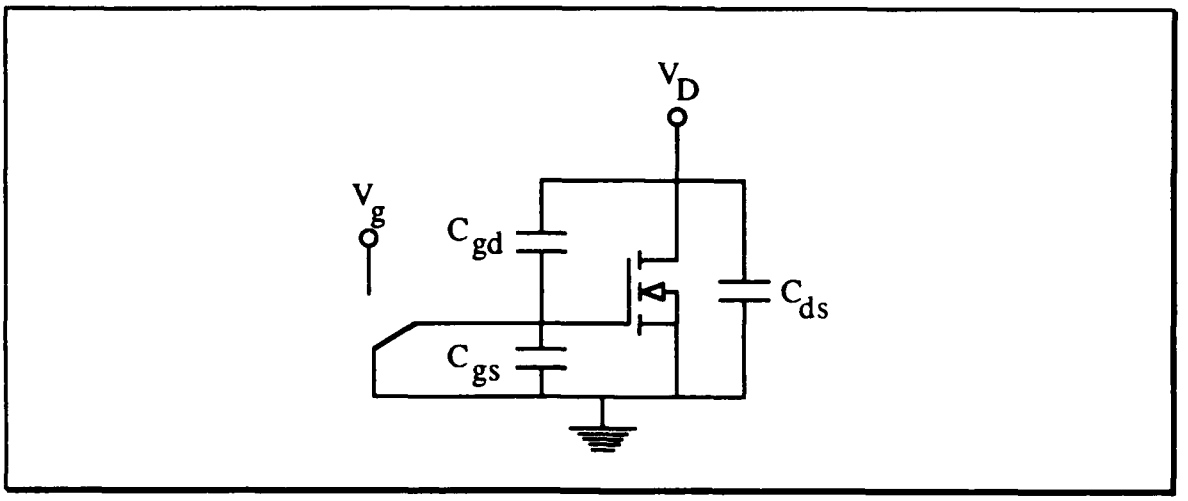

Figure 7. MOSFET capacitive model

If the MOSFET drain potential is a non-zero value, V_D, the drain-to-source, gate-to-drain, and gate-to-source capacitances are charged to $+V_D$, $+V_D$, and 0 volts respectively. When a gate drive is applied to the device, the potentials will change to 0, $-V_g$, and V_g respectively. The net change in voltage across each of the capacitances is $-V_D$, $-(V_D + V_g)$, and V_g. In order to complete the switching action of the MOSFET, the gate drive circuitry must supply the current required to charge both gate-to-drain and gate-to-source capacitances. The requirement of the gate drive circuitry to supply the additional charging current to charge the gate-to-drain capacitance is similar to the Miller effect seen in amplifier circuits. The Miller effect is more on a large signal analysis rather than the small signal analysis usually noticed in typical amplifier circuits. [Ref. 1:p. 94]

When the switch is at a zero potential across the drain-to-source junction and there is no gate drive present, as is the case in the zero-voltage switched converter developed, the capacitances between the gate-to-drain, gate-to-source and the drain-to-source are charged to zero volts. When the gate signal is

applied, the gate-to-source capacitance must charge to the level of the gate drive potential. Since the drain potential is at zero when the switch is turned on, there is no need to charge the gate-to-drain capacitance. In practice, a small coupling will exist between the gate-to-drain and the drain-to-source capacitance in the MOSFET causing a barely noticeable change in the gate drive voltage [Ref. 1:pp. 94-97].

III. CIRCUIT DESIGN

This section describes the details involved in determining the circuit parameters and the techniques used in designing the circuit. The complete circuit schematic is listed in the appendix along with component values.

The PWM controller presently available was the primary engineering design constraint of the regulator due to its limitations in variable frequency operation. The constraint on the design was the inability to operate at a wide range of frequencies due to the reset requirements of the controller. This forced the design to operate in a fixed window of frequencies and pulse widths to allow for operation of the controller in the prescribed area.

A. CONVERTER CIRCUIT DESIGNS

The requirements of a zero-voltage switched converter dictate that the converter must operate in a discontinuous mode. The first parameters chosen in the design are the desired output power and the desired operating frequency. This converter was chosen to transfer 10 watts at a maximum pulse-width of 10 μs. This set the maximum possible operating frequency of the converter to be less then 100 kHz, as determined by the capabilities of the controller to vary its frequency.

The requirement of the controller in zero-voltage switching is that the sum of the on-time and the discharge time be between 10 and 20 μs, and the maximum on-time be limited to 9 μs. With a voltage conversion ratio of 2.8 for 34 volts boosted to 94.7 volts and a 1000 Ω load, a discharge time of 5 μs is obtained.

The total period of the circuit cannot be obtained directly as the frequency varies as the pulse-width changes. As such, an approximate period must be assumed for operation that is in excess of the sum of the switch-on time and the inductor discharge time. The total period is given in equation (28) and was used for iterating the results obtained from the chosen inductor size. Parasitic capacitance values and knowledge of the requirements of the controller to respond to reset cycles are also important in choosing the inductance value and added capacitance.

Once a controller is chosen and the controller's response time to a reset switch is obtained, an initial estimate of the period was made. The controller used in this converter is a Texas Instruments SG3525 PWM controller. Experimental testing indicated a delay of approximately 1 μs after the reset was sent until the gate drive circuit was activated.

As an initial period estimate, the sum of the on-time, discharge time and delay time was used to obtain an estimate for the required inductor size. The initial estimate of the total period was place at 15 μs. This yields an inductance from equation (7) of 538 μH. As a lower range of input voltages would like to be accommodated, a smaller value of inductance was chosen. The desired inductor size was set at 450 μH and built to 467 μH, as described later.

The pass diode was chosen to be a large junction area device. The device chosen was the Motorola MUR 410. The MUR 410 has a peak repetitive reverse voltage of 100 volts and a maximum current-carrying capability of 4 amps at 80 C. The forward voltage characteristics are 0.725 volts at the converter's peak current of 0.6 amps at 25 C. The forward recovery time of the diode is 25 ns. Maximum reverse current at 25 C is 5 μA. The average power

dissipation for the designed operating current of the converter is approximately 0.25 watts. The capacitance of the device decreases exponentially with reverse voltage with the capacitance near 125 pF for a reverse voltage of two volts and drops to an asymptotic value of approximately 35 pF at 50 reverse volts.

The MOSFET used in the converter is the Phillips BUZ 60 power MOSFET. The device characteristics are a maximum voltage rating of 400 volts and a drain-to-source resistance in the on state of less than one ohm. The maximum drain current of the device is 5.5 amps and a maximum power of 75 watts. Typical transconductance is 2.5 amps per volt and the typical drain-to-source capacitance is 30 pF.

Filter capacitors on both the input and output were chosen to maintain a reasonably constant input and output voltage. The value of filter capacitance required is based on the amount of ripple desired in the output. The zero-voltage design operates in a discontinuous mode and the output capacitor is expected to supply the load for the entire time that the switch is on in addition to the dead time. This maximum time is approximately 15 μs. The equation to determine the required capacitor size is

$$C = I \frac{\Delta T}{\Delta V} \tag{33}$$

where ΔT is the time required for the capacitor to supply the load and ΔV is the desired output ripple. For the 1000 Ω load and an output voltage of approximately 95 volts, the required capacitance for a 25 mV ripple is 57 μF. The design value used was 60 μF. As the input of the converter was connected to a regulated dc power supply, the value of the input capacitance was set at 30 μF

since the output capacitance of the source is large. This ensured that a constant voltage source for the converter was available.

Sense resistors were used in the circuit to obtain a control signal for the controller. The desired output voltage was determined by operating the converter in the constant pulse-width variable-frequency mode to determine the parameters for zero-voltage switching. A resistor network of a 91 kΩ and 5.1 kΩ was used as the sense values for the controller with the tap coming off of the 5.1 kΩ resistor to ground.

The schematic of the basic converter design is shown in Fig. 8. The small capacitance placed around the MOSFET, C_{res}, is for proper timing during the resonant ring-down period. Its value is experimentally determined, and it is physically connected directly to the drain and source of the MOSFET to provide a high current path and to minimize the parasitic inductance formed in the wire leads.

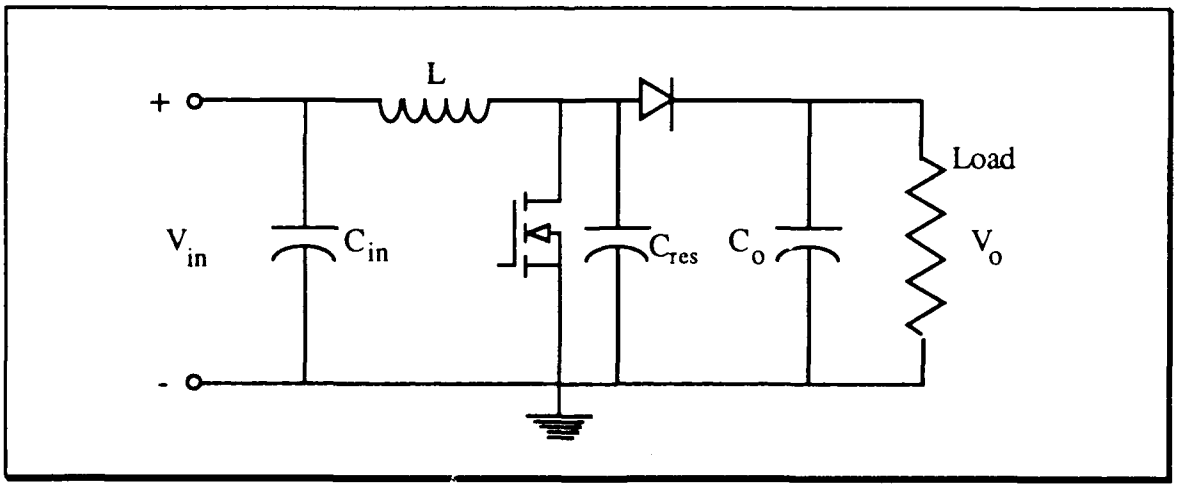

Figure 8. Basic converter schematic

B. CONTROLLER DESIGN

The controller used in the design is the Texas Instruments SG3525 PWM voltage-controlled controller [Ref. 7:p. 3-49 - 3-55]. This controller was chosen for its ability to be synchronized to an external clock. It is a dual output device, but only a single output was used for timing considerations. Figure 9 is a block diagram of the controller used.

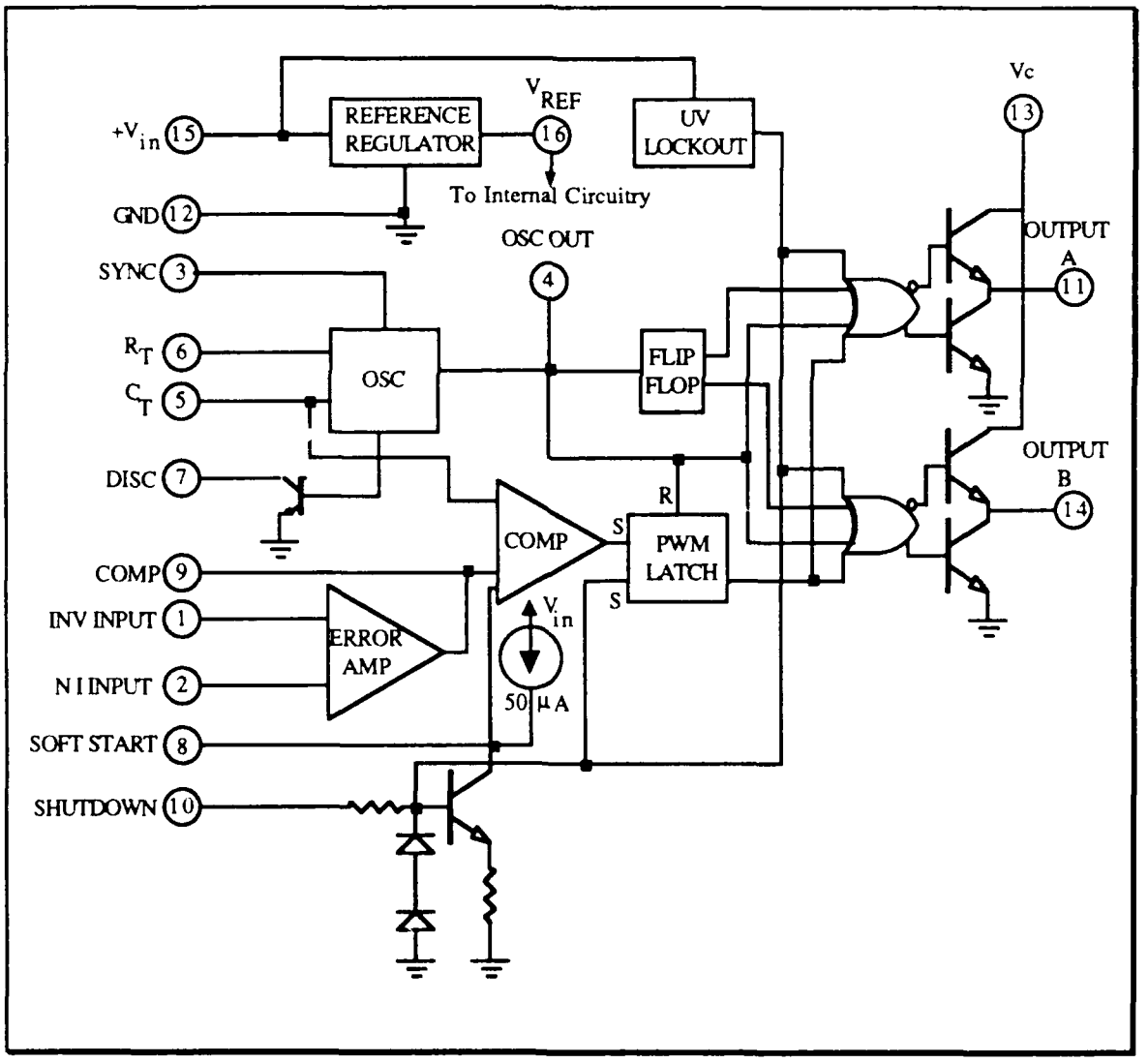

Figure 9. Controller block diagram [After Ref. 7]

Timing for the circuit is critical. The SG3525 controller typical operation allows for the synchronization of the pulse to occur within 10% of the end of the cycle. In order to maintain a wide range of available frequencies for operation, the timing pulse must be able to occur at any reasonable time. For this reason, the device was operated in a quasi-single-ended mode. This mode was accomplished by using one of the available outputs as the driver instead of tying the two outputs together to operate in a single-ended mode. The mode was chosen to allow for the discharge period to end within the timing interval of the unused output. When the reset signal is received on the unused portion of the output cycle, the device ends the conduction period and starts the output cycle used in the converter. When this was accomplished, the available frequency range in the circuit was approximately from a maximum of the single-ended frequency down to the single-ended period plus the required discharge time.

Another difficulty in the timing of the controller is the delay between the time the synchronization pulse arrives and the time the controller re-initiates the gate drive pulse. The delay is due to a minimum voltage level required in the controller's timing circuitry before the pulse is initiated. This time delay is the driving factor in choosing the required size of the added drain-to-source capacitance. The resonant ring-down period must be delayed long enough to allow the controller to respond to the reset pulse while the voltage across the switch is still at zero. If the value of added capacitance is too small, then the resonant period is too short and the voltage will start to rise before the controller can drive the switch into conduction.

The timing in the controller is set by a resistor-capacitor network connected from pins 6 and 5 to ground, respectively. A dead time resistor, R_D, is placed

between pins 7 and 5 to allow for discharge of the timing capacitor after the maximum voltage level in the timing circuitry has been attained. The general timing equation for the controller is approximately

$$f = \frac{1}{C_T(0.7R_T + 3R_D)} . \tag{34}$$

The value for R_D was placed at 10 Ω in this design as a means of limiting noise without affecting the circuit timing. The values chosen in this design for timing are a timing resistance of 3.9 kΩ and a capacitance of 0.005 μF. This sets the frequency of operation at 72.5 kHz.

The controller has the ability to drive the gate directly without additional drive circuitry. This allows for fewer components in the gate drive circuitry, although separate drive circuitry could be used to drive the gate faster into saturation speeding up the turn-on and turn-off transient periods.

Feedback in a boost circuit is required in the controller due to an inherent time delay in the operation of the converter. This time delay is created because the actual transfer of energy through the converter takes place during the period when the switch is opened vice closed. This requires that the controller be operating on an average sense value vice an instantaneous value to allow for proper pulse-width determination of the converter. Feedback is accomplished using a dual feedback system of a lowpass RC network to the inverting terminal and a capacitor from the output of the error amplifier to ground. This stabilizes the system and allows for a regulated output with varying loads and input voltages within the constraint of the operating frequencies of the controller. The capacitor to ground tends to short the high frequency switching noise effects of the converter to ground, stabilizing the converter from switching noise

transients. The RC filter in the feedback loop acts as an integrator and slows the system response to the output of the error amplifier. This feedback tends to reduce the frequency response of the converter to approximately two decades below the switching frequency.

The feedback values chosen in this design are a feedback resistor of 100 kΩ in series with a capacitance of 0.68 μF and a capacitance of 0.02 μF to ground. This successfully stabilized the system to switching noise as well as load and input variations.

C. MAGNETIC COMPONENT DESIGN

The magnetic component used in the converter is a single toroidal inductor manufactured by Amidon Associates of North Hollywood, Ca. The core is designated as T3-130 and is used for inductors that operate up to 600 kHz with an A_L value for the core of 350 μH/100 turns. To obtain the number of turns required for the device,

$$\text{Turns} = 100\sqrt{\frac{\text{desired L } (\mu\text{H})}{A_L\ (\mu\text{H}/100\text{ turns})}}\ . \tag{35}$$

The desired circuit inductance was 450 μH, and the coil was wound with 114 turns of magnetic wire. The measured inductance was 467 μH.

D. DRAIN VOLTAGE SENSING CIRCUIT

A technique for sensing the drain potential is required if the desire to switch the MOSFET near zero volts is to be met. The controller's response, however, is too slow as a result of its internal design. This requires that the signal for resetting the controller be sent prior to the drain potential reaching zero. In this design, the reset signal is taken from the changing inductor voltage.

An additional 10 turn winding was placed on the core with additional wire creating a small step-down transformer for use as a voltage sense for the inductor. This winding had one side placed at system ground and was used to determine when the core had an inflection point in voltage for use in the zero-crossing detector circuitry. The discharge period is set to be the positive excursion and the charge period produces the negative excursion in the voltage waveform.

The time that the signal is sent to reset the controller is approximately at the inflection point of the inductor voltage during the resonant ring-down period. This inflection occurs at the time when the voltage across the switch equals the input voltage. This voltage is half-way between the peak value and the minimum value of voltage seen by the switch if the body diode does not conduct. With the value chosen for the additional circuit capacitance, this time is approximately 500 ns after the inductor discharges and the pass diode turns off.

The transformer action of the additional windings on the converter inductor provides a signal that follows the inductor voltage at all points in time. When one side of the winding is grounded, the signal becomes ac with the zero crossing occurring near the point of inflection of the resonant ring-down cycle. When the controller time lag is taken into account, the reset pulse for the controller must occur at a time that precedes the drain potential from reaching zero. Figure 10 is a schematic of the inductor voltage sensing circuit.

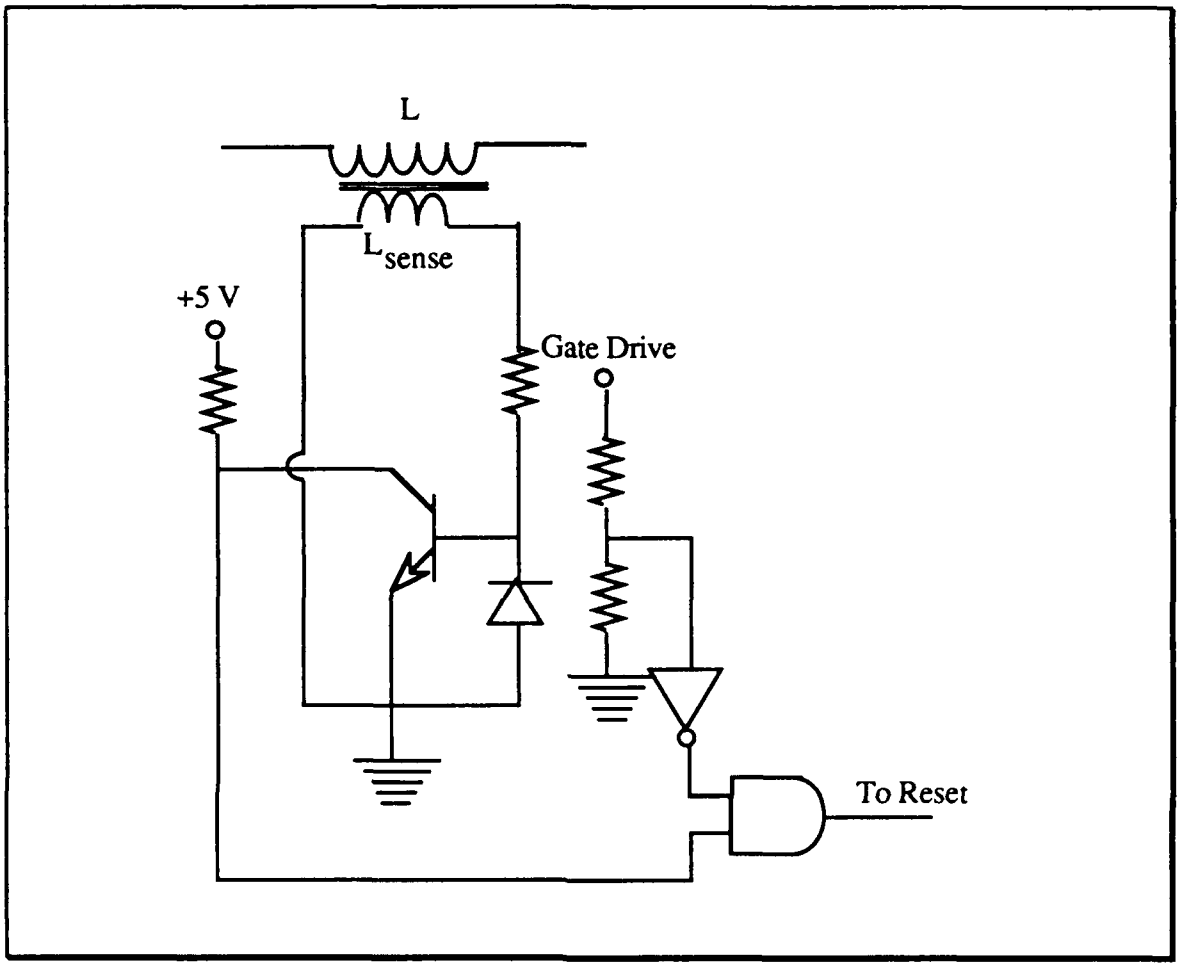

Figure 10. Inductor voltage sensing circuit

The base of a high speed switching transistor is connected to one end of the transformer winding. When the zero crossing occurs in the secondary of the transformer, the transistor will saturate sending a five volt signal to the logic circuitry for the reset pulse. The base is connected to ground via a diode to prevent the possibility of the transistor's base-emitter junction from going into zener breakdown during reverse bias periods.

A pulse for the reset circuit is generated when the transistor is saturated and the gate drive voltage is not present. This prevents a pulse from occurring when

the gate drive is present and disrupting the controller. The logic for the reset trigger pulse is

$$\text{trigger} = Q \bullet \overline{\text{drive}} \tag{36}$$

where Q is the output of the transistor and drive is the gate drive voltage.

E. CIRCUIT LAYOUT REQUIREMENTS

Layout of a power converter circuit is an important task. The high current paths and critical timing elements must be identified and an effort must be made to reduce the length of the leads going to these elements. Any excess lead lengths will result in parasitic inductance and cause ringing in the circuit when switching action occurs.

The common ground point of the circuit for all elements connected to ground is at the source of the MOSFET. This prevents ground loops from being present, possibly causing instability in the control loop. In addition, the wires of the sense resistor must be intertwined to ensure that a loop is not available for inductive pick-up of the generated transient noise in the circuit.

The capacitance added to the circuit for timing enhancement must be connected as close as possible to the drain and source with very short leads. This prevents the inductive nature of the capacitor from resonating during the switching periods and provides a high current path around the MOSFET during turn-off.

The noise reduction techniques required in the controller circuitry are a capacitive network on the power supply and a small resistance between the chip power and the output drive power. The values for capacitive filtering are a large 6.8 μF tantalum capacitor in parallel with a small 0.68 μF ceramic

capacitor connected from the point of entry of power into the controller at pin 15 to the ground at pin 12. This resulted in a large reduction in the amount of switching noise that was present in the circuitry from affecting the controller. A 10 Ω resistor was placed between the controller power on pin 15 and the output drive power on pin 13 to limit the amount of switching noise being placed back into the system. A 0.68 μF capacitor was placed between pin 15 (output drive power), and pin 12 (ground), to reduce the noise at that point in the controller. These noise reduction techniques are vital to the proper operation of high-gain high-frequency controllers. [Ref. 8:pp. 39-43]

IV. EXPERIMENTAL RESULTS

A zero-voltage switched variable-frequency PWM converter was designed and tested in this thesis. The device operated at a nominal 67 kHz and 8 μs pulse-width for a regulated conversion of 35 volts to 94.7 volts delivering 8.87 watts operating at 93.5% efficiency. As the input voltage varied between 33.5 and 41.8 volts, the frequency range was from 60 kHz to 80 kHz with pulse widths ranging from 10 μs to 6 μs. The converter was first designed and tested in a constant pulse-width variable-frequency mode to determine the required timing for the circuit. By operating in this mode, it was possible to determine the proper voltage conversion ratio range for the zero-voltage switched mode. The device was operated with a pulse-width of 8 μs and the frequency was varied in an open loop configuration to obtain the zero voltage condition. The output voltage obtained when operating in this condition with a 35 volt input was 95 volts with a 1000 Ω load.

After the parameters of the circuit were measured, the frequency controller was replaced by a PWM controller operating with a maximum pulse-width of 10 μs. The feedback loop was closed and an output voltage of 94.7 volts was obtained while operating in a zero-voltage switched mode.

Various circuit parameters for an input voltage of 37 volts boosted to 94.7 volts were measured and are listed below:

- $t_{on} = 7.4\ \mu s$,
- $t_r = 0.1\ \mu s$,
- $t_d = 4.8\ \mu s$,
- $t_f = 1.2\ \mu s$,

- $t_{bd} = 0.5\ \mu s$,
- $I_p = 0.6$ amps,
- $T = 14\ \mu s$.

The average input current was 256 mA at 37 volts and the output values are 93.7 mA at 94.7 volts. The output power is 8.87 watts with an input power of 9.47 watts resulting in circuit losses of 0.6 watts. These losses are diode losses, inductor losses, MOSFET conduction losses, transient switching losses, capacitor leakage and sensing circuit losses. Accountable losses are 0.25 watts in the pass diode and 93 mW in the sense resistors. The conduction losses are approximated from the 1 Ω resistance of the MOSFET and the rms current through the device. The conduction losses are calculated from

$$P_{cond} = \frac{1}{T} \int_0^{t_{on}} R_{ds\text{-}on}\, i^2(t)\, dt \ . \qquad (37)$$

The instantaneous current is a linear function starting at zero amps and rising to a peak value of 0.6 amps at the end of time t_{on}, 7.4 μs. The losses experienced in the channel during conduction are 63.4 mW. The sense circuit voltage levels range from 5.1 volts during discharge to –3 volts during inductor charge. This average voltage in the sense circuit, 4 volts, is dissipated across the 1 kΩ resistor resulting in a dissipation of approximately 16 mW. This leaves approximately 178 mW of other losses.

Assuming the circuit inductance is equal to the inductance of the main inductor used in the circuit, the parasitic and added circuit capacitance was obtained from the ring-down period of 1.2 μs. The resulting value can then be used to validate the derived equations. Using equation (21) with the input and utput voltages obtained, the value for the total average circuit capacitance is

600 pF. Of this value, 390 pF was added to obtain the required timing for the controller. This yields an average parasitic capacitance for the circuit of 210 pF.

Using the value for total average circuit capacitance, the times for other portions of the circuit are calculated and checked against observed values. The rise time for the circuit is given by equation (15). The calculated value for rise time is 0.1 μs which compares with the observed value. The discharge time is obtained from equation (16). For a peak current of 0.6 amps, the calculated discharge time is 4.8 μs. Again, this compares favorably with the measured value. Equation (24) is used for determining the body diode conduction time. When calculated using the total average capacitance value, a conduction time of 0.63 μs is obtained vice the measured 0.5 μs. The disparity between the calculated and observed value are due to the losses during ring-down, which reduce the peak current through the inductor when the body diode starts conducting, as well as the effect of varying capacitance in the pass diode and the MOSFET as the circuit potentials change.

Photographs were taken of various current and voltage waveforms in the circuit to illustrate the technique and the results obtained for the zero-voltage switched boost converter.

Figure 11 is the drain voltage waveform of the converter operating in a constant pulse-width variable-frequency mode. Scaling in the photograph is 20 volts per division and 2 μs per division. The rapid rise in voltage occurs when the switch is turned off and the switch voltage rises to the output voltage level. When the inductor has been depleted of energy, the diode blocks current flow from the output and the resonant nature of the converter is readily observed. The switch is turned on and the voltage drops rapidly to zero. The

energy dissipated in the switch at turn-on is proportional to the square of the voltage level.

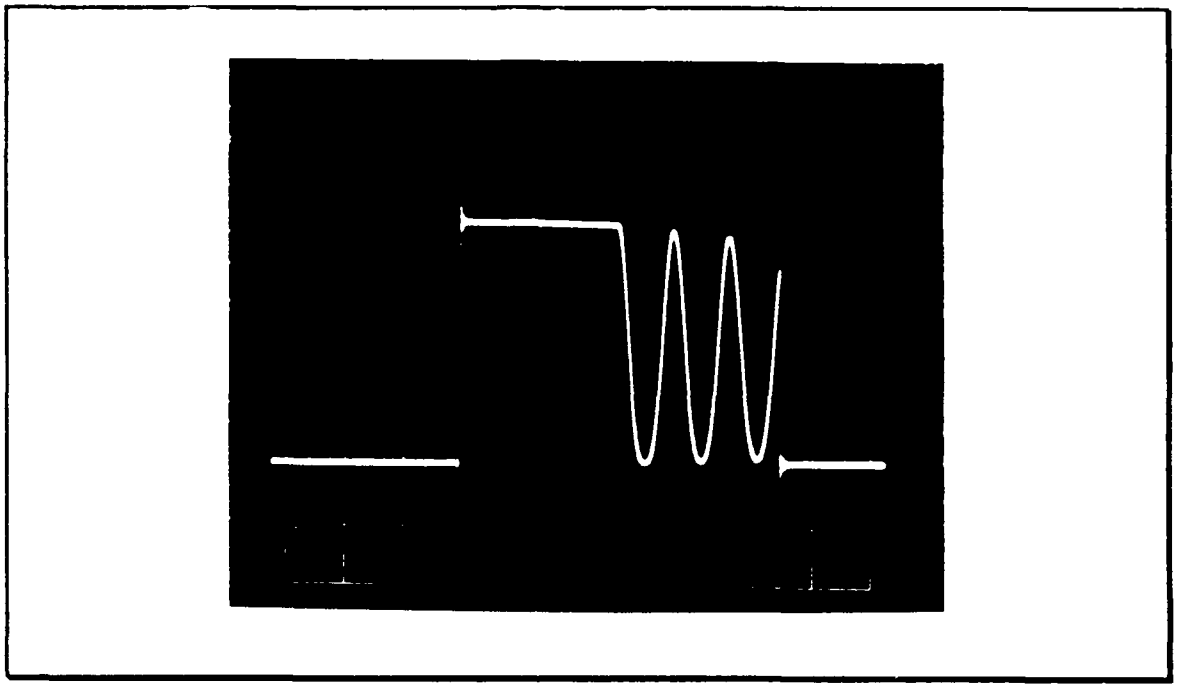

Figure 11. Drain voltage illustrating resonant property

The top trace of Fig. 12 is the gate drive pulse at 5 volts per division and the bottom trace is the drain voltage at 50 volts per division and 2 μs per division. The ringing noticed in the gate drive pulse on the rising edge, the falling edge, and after is due to the excess gate drive lead lengths used to accommodate the insertion of a current probe. The extra inductance of the lead in combination with the gate capacitance was sufficient to cause oscillations in the gate drive, and could possibly lead to instabilities in switching. Of particular note in the gate drive waveform is the lack of any ringing at the top of the pulse. This is a result of the minimal amount of energy required to turn the MOSFET on because of the zero-voltage switching technique. The resonant ring-down cycle of the drain voltage is evident along with the clamping effect near zero volts. The gate drive

is applied when the voltage at the drain is at the minimum value and does not allow for the voltage to ring back up towards the output voltage level as illustrated in Fig. 11.

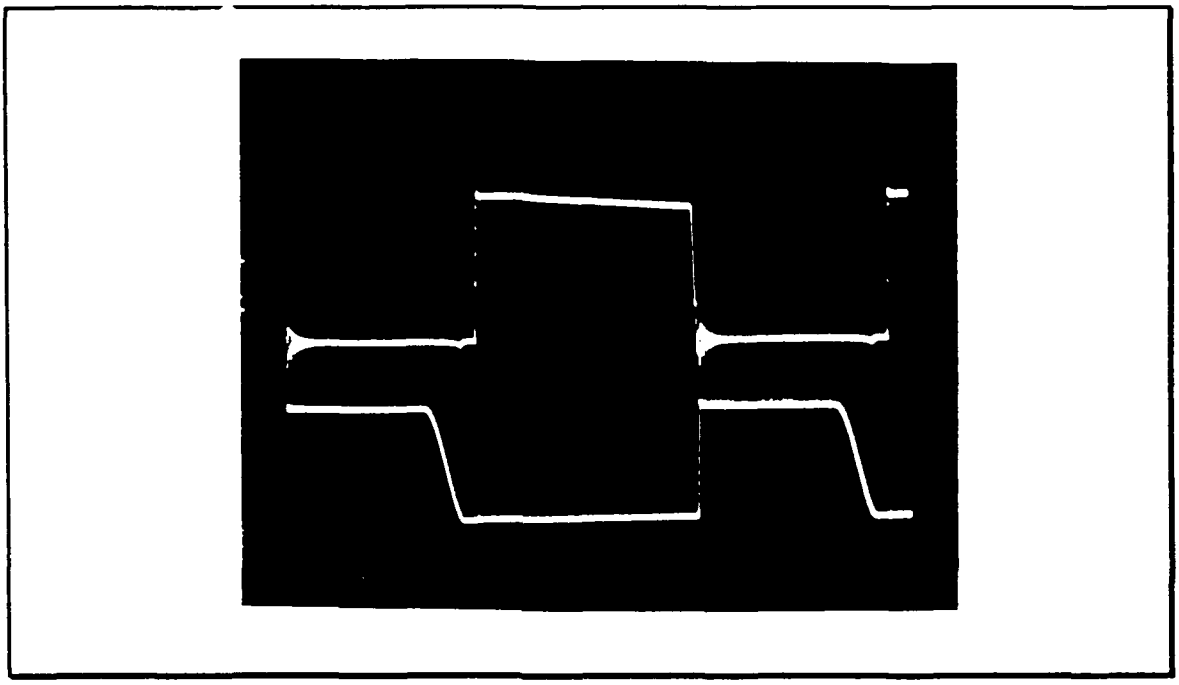

Figure 12. Gate drive and drain voltage

Figure 13 is a combination of the gate drive at 5 volts per division and the sum of the current through the MOSFET and added capacitance at 0.2 amps per division and 2 μs per division. The beginning portion of the current trace illustrates the period when the switch is not conducting. A resonant current sinusoid is visible after the inductor has been depleted of energy. At this time, the energy stored in the capacitance is transferred back to the inductor and source. The minimum in the current waveform is the point of inflection in the drain-to-source voltage. The resonant cycle continues until the voltage across the capacitance forward biases the body diode, at which point the voltage is clamped and the inductor continues discharging into the source. The discharge at this

point is linear and will continue until the energy has been transferred into the source.

The switch is turned on when the drain voltage is zero and the body diode is still conducting. In the case of this converter, the turn-on occurs when the current has just been depleted in the inductor. A continual linear slope is maintained throughout the cycle from the commencement of the body diode conduction region to the peak current at the end of the on-time of the switch at a peak value of approximately 0.6 amps. The turn-off transient noise is visible as the current through the switch falls to zero. This is a result of the high capacitance value of the pass diode resonating with the MOSFET capacitance and inductance.

An important point to note in determining the pulse-width of the converter, is that the gate drive can occur at any time that the body diode is conducting. A dead time in the converter is created when the inductor is discharging through the body diode of the MOSFET. The inductor is discharging linearly through the body diode and will discharge at a rate that is determined by the size of the inductor. Therefore, the gate drive can occur at any time during the body diode conduction time, but the actual effective pulse-width does not commence until after the inductor has completely discharged into the source.

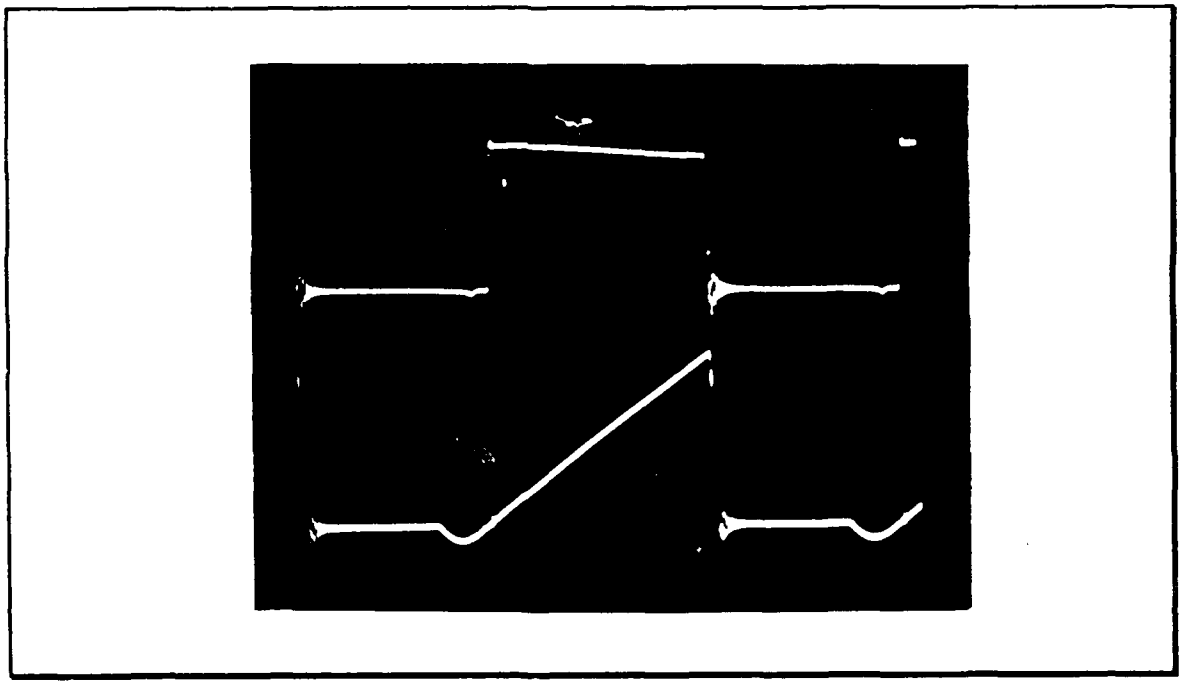

Figure 13. Gate drive and switch current

Figure 14 is the gate drive and the inductor current. The scaling for the photograph is the same as in Fig. 13. This figure illustrates the linear charge and discharge cycle of the inductor and the dip in the negative current direction during the period of time when the inductor and capacitor are resonating through the time of body diode conduction. The turn-on transition in the inductor occurs as the current flow is about to reverse direction causing the voltage at the drain to rise.

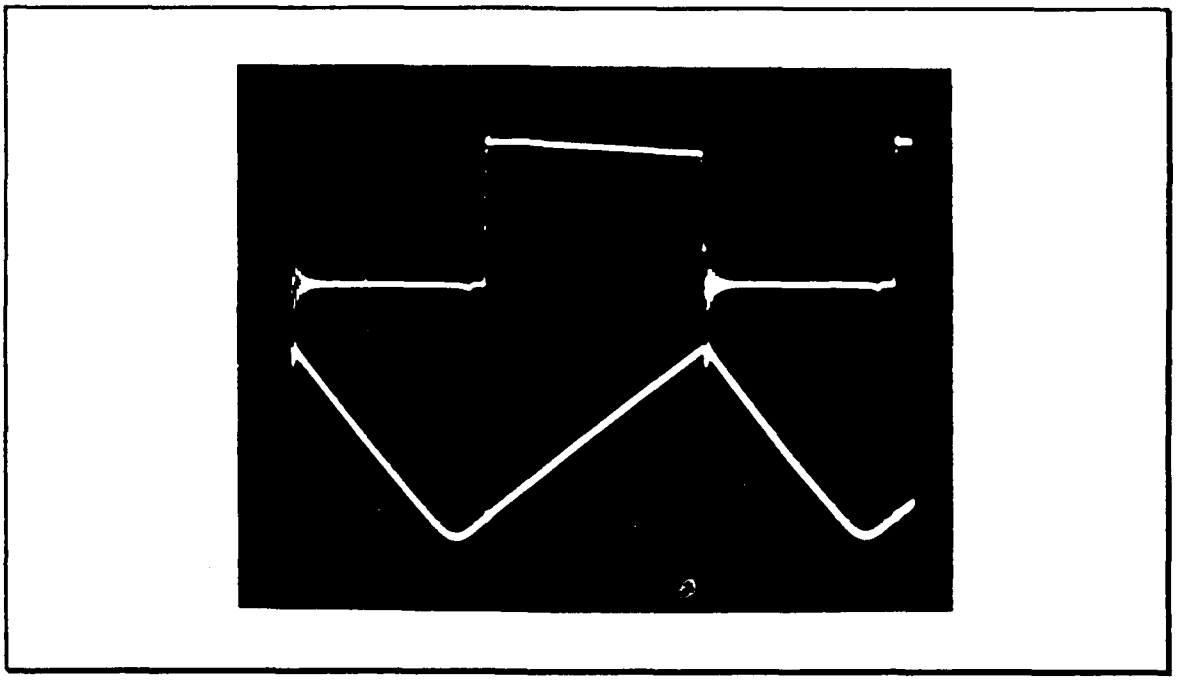

Figure 14. Gate drive and inductor current

Figure 15 is a photograph of the drain potential and the output current to the filter capacitor. Drain voltage is measured in 50 volts per division and diode current is 0.2 amps per division at 2 μs per division. As the switch is opened, the voltage at the drain rises and the diode starts to conduct. The noisy conduction beginning is also seen in Fig. 13 where the drain current oscillates at turn-off. The parasitic inductance in the long leads and the devices parasitic capacitance are responsible for the resonating action during the transition periods.

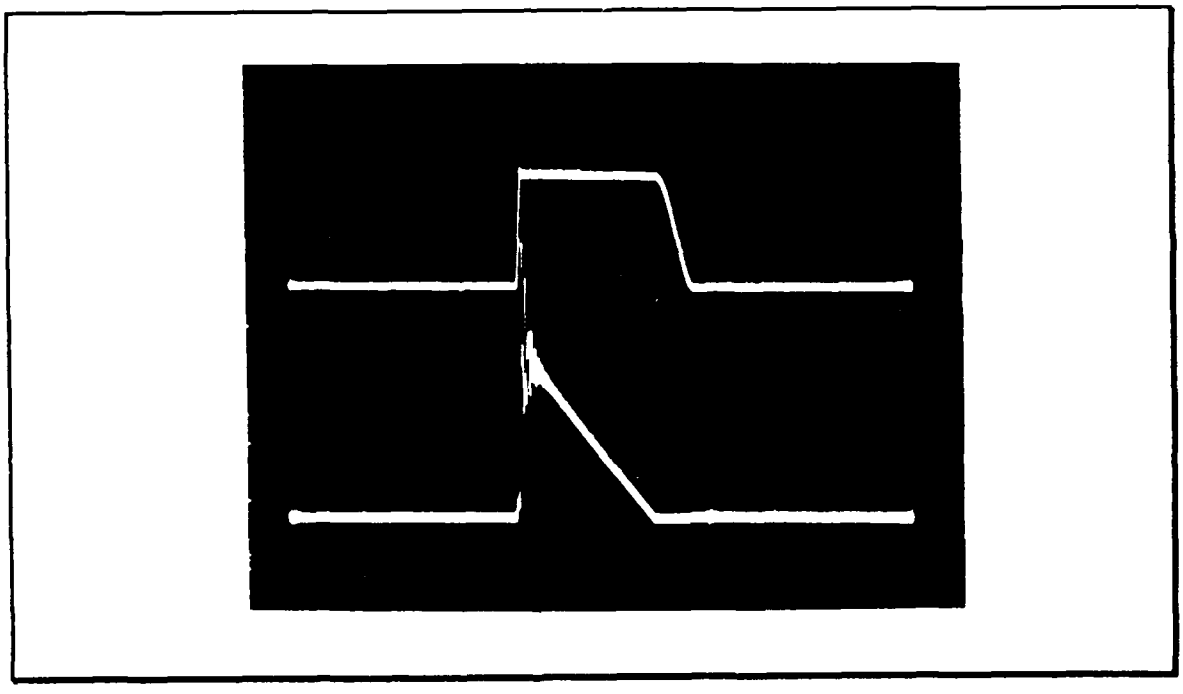

Figure 15. Drain voltage and diode current

Figures 16 is a photograph of the drain voltage and the reset pulse. The reset pulse ends when the gate drive begins. The scaling is 2 volts per division for the reset pulse and 50 volts per division for the switch voltage waveform at 2 μs per division. The width of the reset pulse is the delay in the controller from the beginning of the reset pulse to the application of the gate drive.

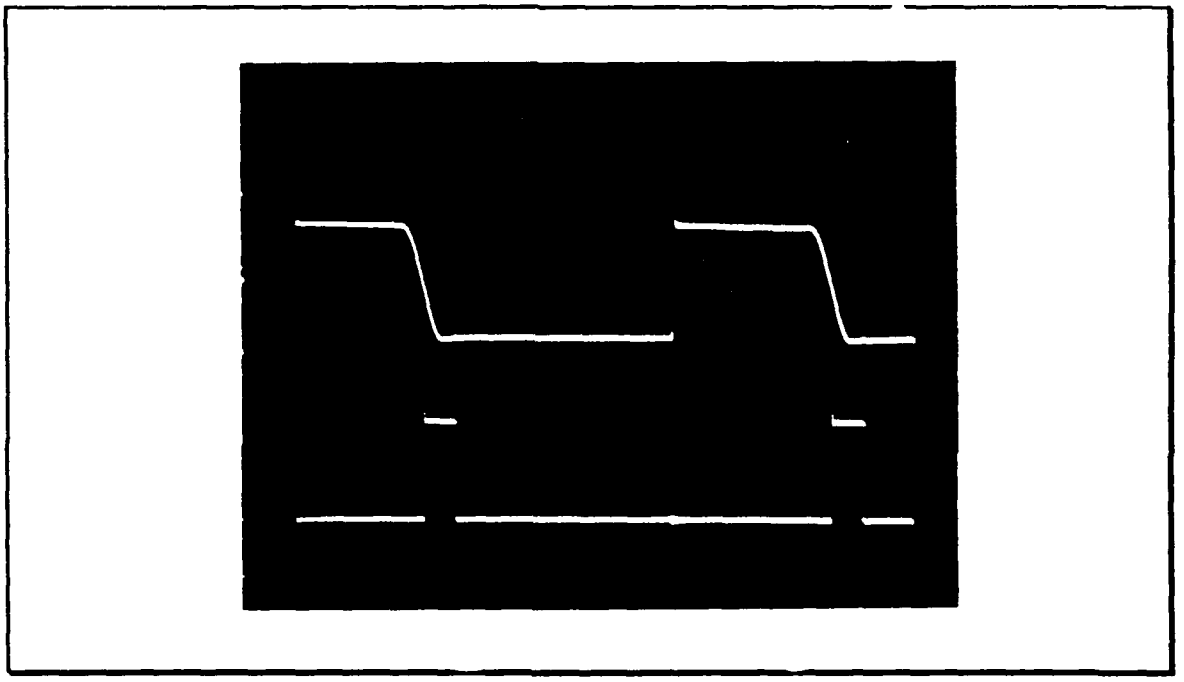

Figure 16. Reset pulse and switch voltage waveform

Figure 17 is a photograph of the reset pulse and the timing waveform of the controller. The timing voltage is measured at 1 volt per division and the reset pulse is 2 volts per division at 2 μs per division. The full sawtooth waveform is the portion of the controller that is used in driving the power MOSFET. The incomplete sawtooth is the portion of the cycle that is interrupted by the reset pulse for the zero-voltage implementation of frequency variation.

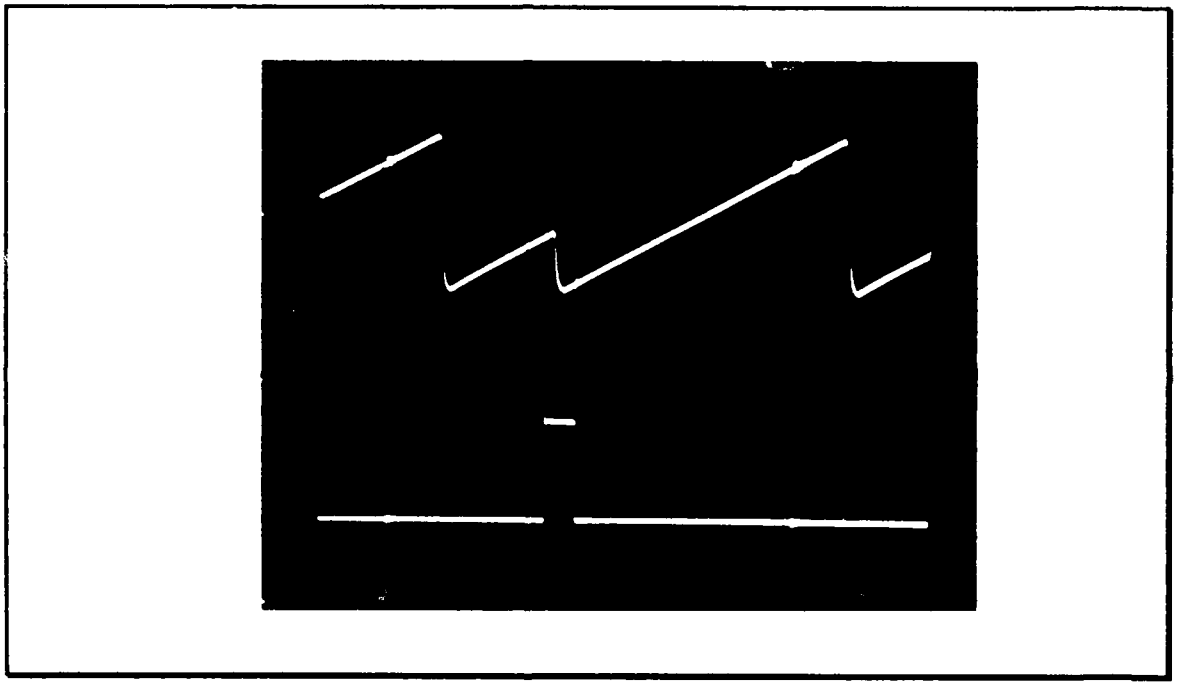

Figure 17. Reset pulse and timing waveform

Figure 18 is a photograph of the timing pattern and the gate drive illustrating the relationship between the gate drive and the controller timing. The scaling is 5 volts per division for the gate drive and 1 volt per division for the timing waveform at 2 μs per division. The delay between the end of the short ramp and the beginning of the gate drive requires that the reset pulse be sent prior to the actual zero crossing of the drain potential.

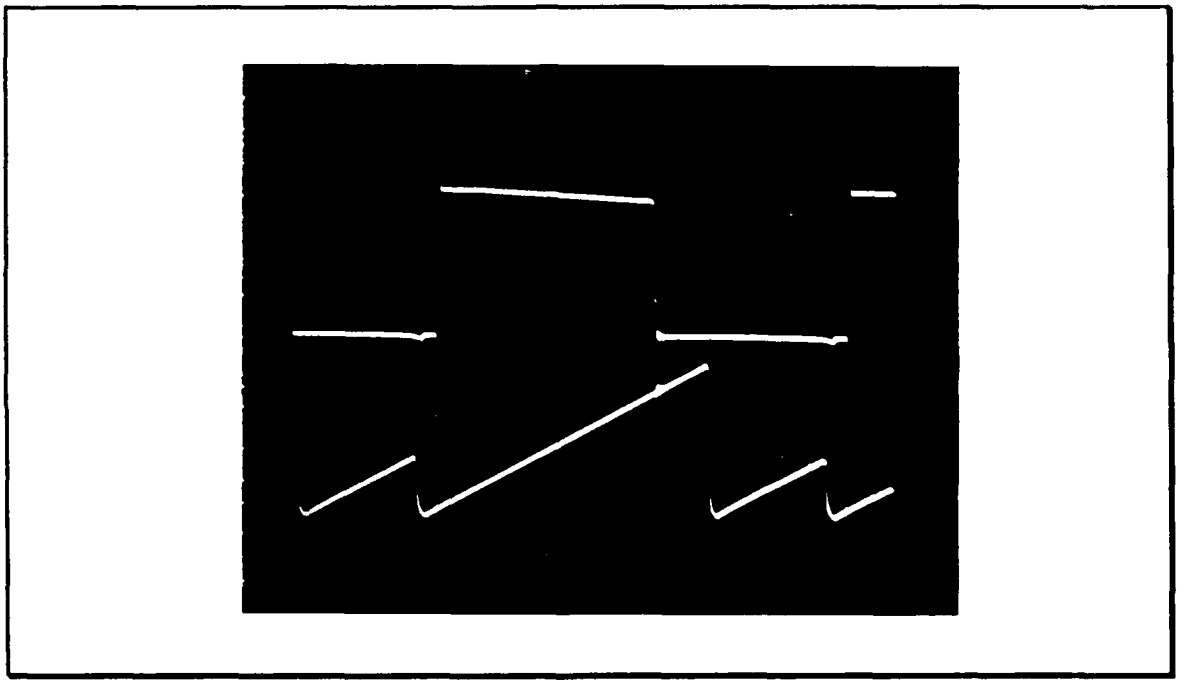

Figure 18. Gate drive and timing waveform

Figure 19 illustrates the charge removal during turn-on and turn-off of the MOSFET by the controller. The bottom trace is the gate drive voltage and the top trace is the gate drive current. Scaling is 5 volts per division and 0.2 amps per division at 1 μs per division. The turn-on pulse is free of oscillatory noise as it is switched when there is no charge stored in the capacitance of the device; the turn-off pulse has noise as a result of turning the MOSFET off under load.

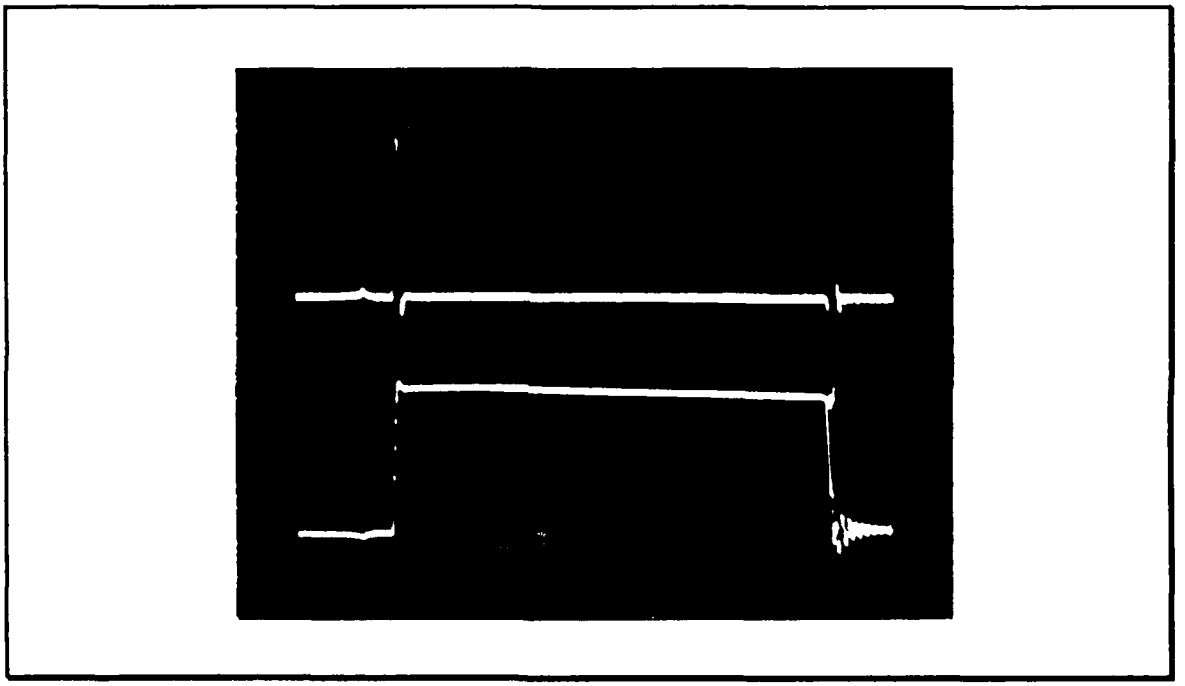

Figure 19. Gate drive voltage and drive current

V. CONCLUSIONS

The variable-frequency pulse-width-modulated boost regulator developed in this thesis will allow for operation of PWM boost converters at very high frequencies without transient turn-on losses. The technique utilizes a frequency control scheme where the characteristics of the controller for the converter are altered to cause switching to occur when the voltage at the drain of the MOSFET is near zero volts. In addition to reducing transient turn-on losses, zero-voltage switching reduces noise generation in the circuit and simplifies the gate drive requirements.

Other characteristics of optimal switch utilization are met in addition to turning the switch on under a zero drain-to-source potential. These include:

- Maximum peak voltage across the switch is limited to the output voltage level.
- Peak and average currents through the switch are proportional to output power requirements.

This is currently the only converter with these characteristics. The zero-voltage switched quasi-resonant converter operates with zero-voltage switching, but the current through the switch is constant based on the maximum load requirement, and the voltage across the switch is twice the output voltage level.

This converter design was built and tested. The design operated in a frequency range from 60 to 80 kHz with pulse widths of 10 to 6 μs delivering 8.87 watts at 93.5% efficiency with an input voltage of 35 volts boosted to 94.7 volts. The primary engineering constraint on the circuit is the inability of

the controller to operate in a variable-frequency mode in addition to its normal PWM controller mode.

Further research into this area includes designing a controller that could be frequency modulated in addition to being pulse-width modulated. This is critical if the technique for combined frequency and pulse-width control is to be used to regulate a load over a wide range of input voltage levels and output load requirements. Some desirable characteristics of this controller are:

- The maximum pulse-width is much longer then the normal desired operating pulse-width to allow for load and input voltage variations. No constraints are placed on the timing of the reset pulse during the timing interval.
- Sense lead for determining the drain potential. When the potential is at zero volts with no gate drive present the timing pulse will restart. Ideally this timing pulse should have no delay to the commencement of the gate drive when the zero is sensed. Realistically, the timing will most likely be obtained from the inductor and any time lag that is present can be used for the delay from the inductor signal to the point when the voltage at the drain reaches zero.
- High gain error amplifier with available feedback for stability.
- High current output for driving the power MOSFET directly.

The technique developed in this thesis will provide power converter designers with an alternative for designing high-frequency converters with minimal transient losses and switch stresses. This will allow for smaller reactive components, producing higher power density converters, and will increase the transient response of the regulated converter.

VI. APPENDIX

The following schematic is the final engineering design that performed the operation of zero-voltage switching in a boost dc-dc regulated converter producing 94.7 volts. Part components are as follows:

V_{in} = 33-42 volts
C_{filter} = 30 μF
L = 467 μH
L_{sense} = 10 turns
D_1 = MUR 410
D_2 = 1N914
Q_1 = BUZ 60
Q_2 = 2N3252
Q_3 = 74LS04N
Q_4 = 74S08N
R_1 = 91 kΩ
R_2 = 5.1 kΩ
R_3 = 510 Ω
R_4 = 1 kΩ
R_5 = 10 kΩ
R_6 = 10 kΩ
R_7 = 150 Ω
R_8 = 10 kΩ
R_9 = 2.7 Ω
R_{10} = 10 Ω
R_{11} = 3.9 kΩ
R_{12} = 100 kΩ
R_{load} = 1 kΩ

C_1 = 0.005 μF
C_2 = 0.68 μF
C_3 = 0.02 μF
C_4 = 0.08 μF
C_5 = 0.68 μF
C_6 = 0.68 μF
C_7 = 6.8 μF
C_8 = 0.68 μF
Controller = SG3525
Required Power = 12, 5 volts

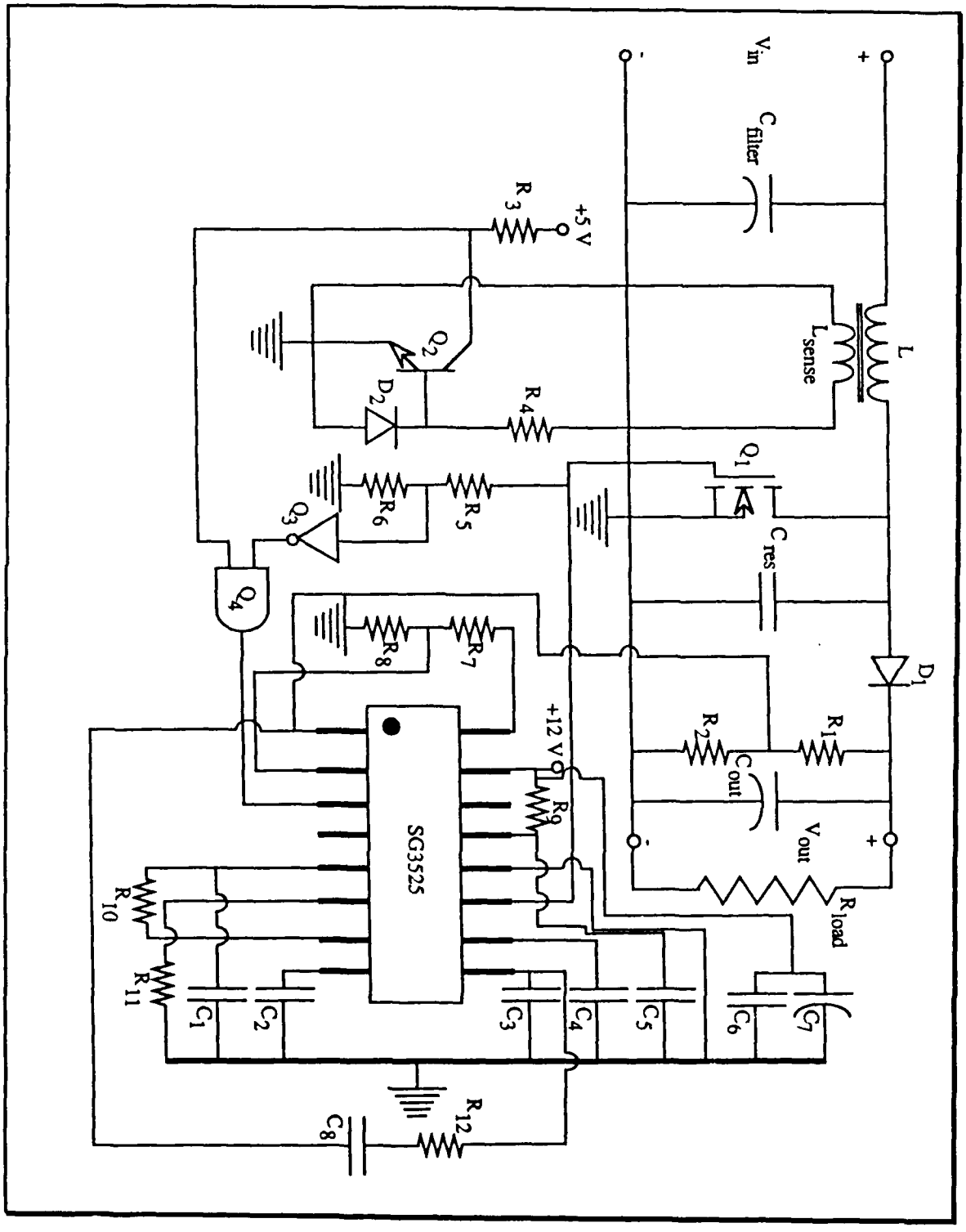

Figure 20. Complete Circuit Schematic

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